AUTOMOTIVE, Analog-Front-End IC for resistive bridge sensor

MV3830ARREG2 Datasheet

DESCRIPTION

MV3830 is an Analog Front-End IC which changes an analog signal output from a sensor to a digital signal, processes the digital signal, and outputs it to a host such as a microcomputer in the subsequent stage through digital communication. This is compatible with a wide variety of sensors.

FEATURES

- Analog power supply：2.2V to 5.5V
- Voltage regulator for external sensor (1.8V)
- Offset cancel circuit for external sensor
- Low noise Programmable Gain Amplifier (1 to 128)
- External sensor power off switch
- 24bits⊿ΣADC with a wide dynamic range is mounted
- Internal temperature sensor
- Time-dependent change correction function
- Offset TC and gain TC correction
- Non-volatile memory for corrective coefficient of sensor
- I/F:I2C Fast Mode (400kbps) + CRC(optional)
- Change AD conversion rate
- Configurable IRQ output with threshold value
- AEC-Q100 Grade2 Temperature range: -40deg.C to +105deg.C
- Self-check function
  Sensor open/short detector
  Power supply low voltage detector
  Current limit for VRG terminal
  NVM CRC

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BLOCK DIAGRAM

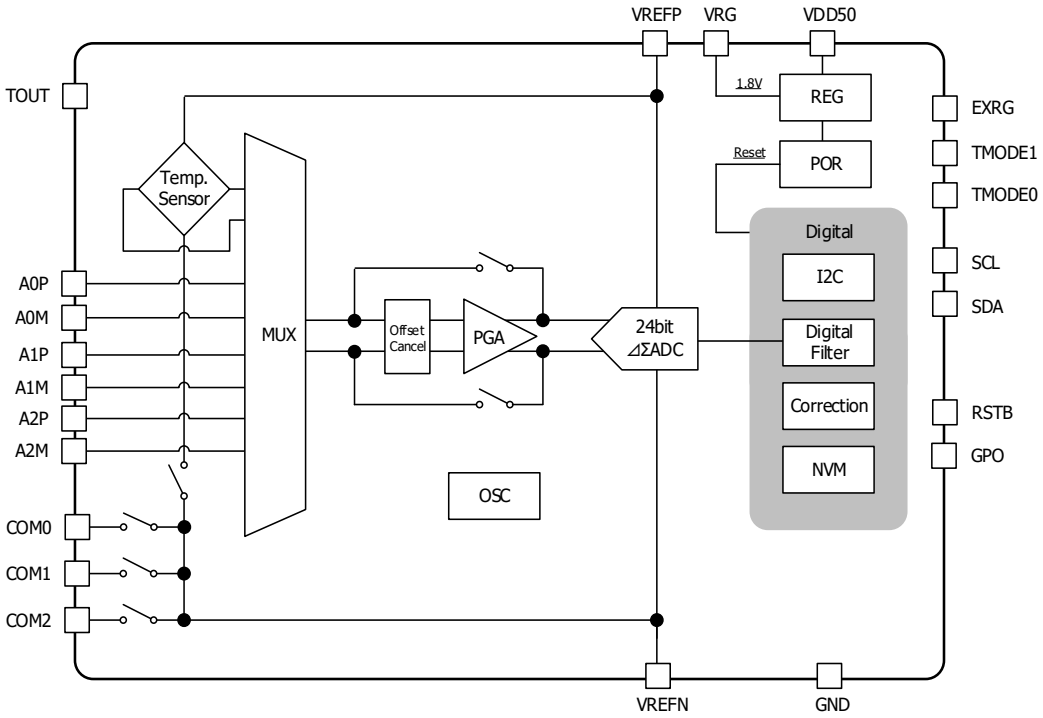


Fig. 4.1 Block diagram

PIN CONFIGURATION

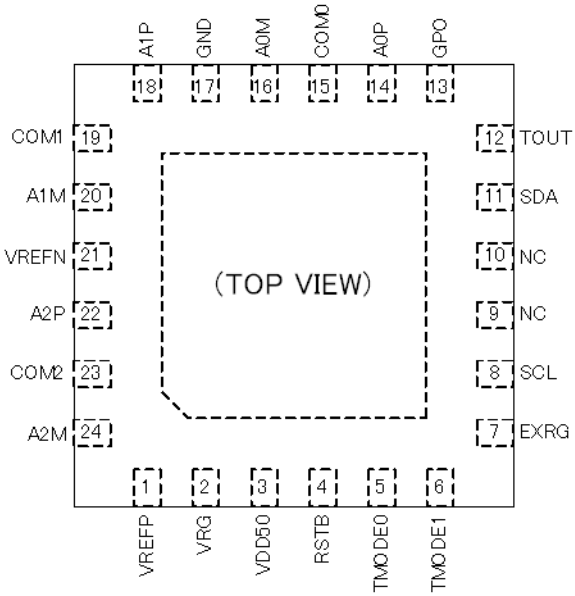


Fig. 5.1 Pin configuration (Top view)

TERMINAL EXPLANATIONS

Function of the pins

Table. 6.1 Pin table

No.	Name	TYPE	FUNCTION
1	VREFP	I	Reference voltage plus
2	VRG	I/O	EXRG = ”Low”: Internal regulator output EXRG = ”High”: Power supply, Drive voltage for external sensor Need external 0.1uF capacitor
3	VDD50	-	Power supply for 5V Need external 1.0uF capacitor
4	RSTB	I	Negative logic reset(Built in pull-up)
5	TMODE0	I	Setting for TEST mode(Built in pull-down)
6	TMODE1	I	Setting for TEST mode(Built in pull-down)
7	EXRG	I	Setting for VRG input mode(Built in pull-down) (“Low” : Internal regulate, “High” : External VRG input)
8	SCL	I/O	Serial clock for I2C
9	NC	-	No connection
10	NC	-	No connection
11	SDA	I/O	Serial data for I2C
12	TOUT	O	Output port for analog test Output signal for VDD50 voltage detect (default setting)
13	GPO	O	General purpose output port (Built in 80k ohm pull-down)
14	A0P	I	External temperature sensor input signal plus: Channel 0
15	COM0	O	Pin for controlling external temperature sensor ground: Channel 0
16	A0M	I	External temperature sensor input signal minus: Channel 0
17	GND	-	Ground
18	A1P	I	External sensor input signal plus: Channel 1
19	COM1	O	Pin for controlling external sensor ground: Channel 1
20	A1M	I	External sensor input signal minus: Channel 1
21	VREFN	I	Reference voltage minus Connect with GND
22	A2P	I	External sensor input signal plus: Channel 2
23	COM2	O	Pin for controlling external sensor ground: Channel 2
24	A2M	I	External sensor input signal minus: Channel 2

Equivalent circuit of the pins

Table 6.2 Equivalent circuit of the pins (1/3)

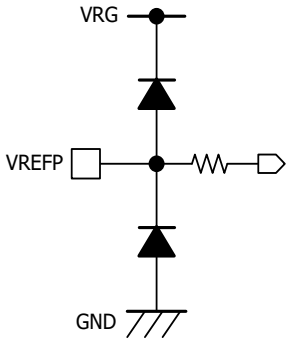
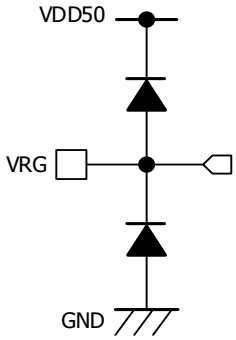
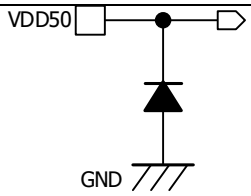
Pin name	TYPE	Equivalent circuit
VREFP	I	
VRG	I/O	
VDD50	I	

Table 6.3 Equivalent circuit of the pins (2/3)

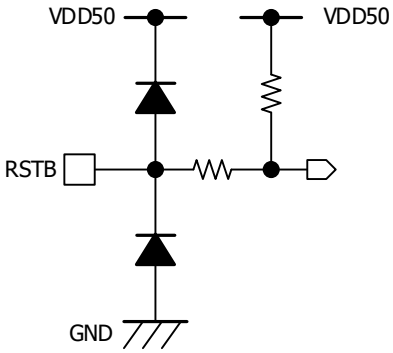
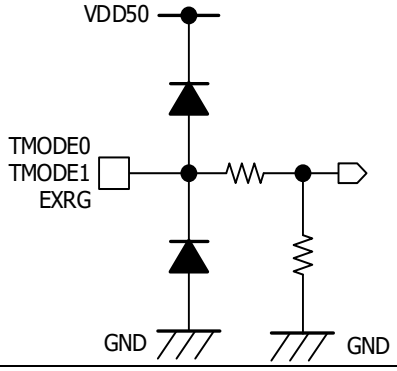
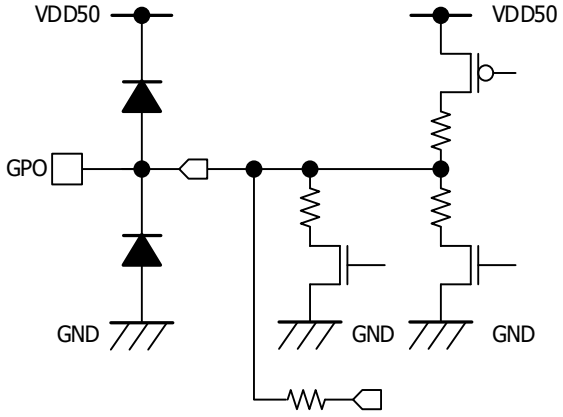
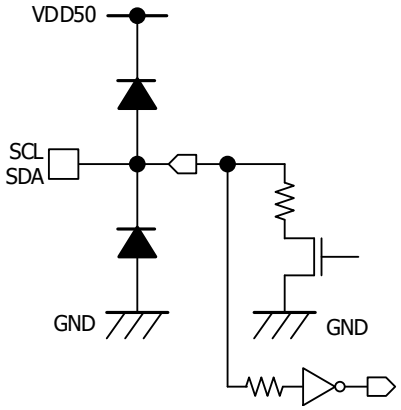
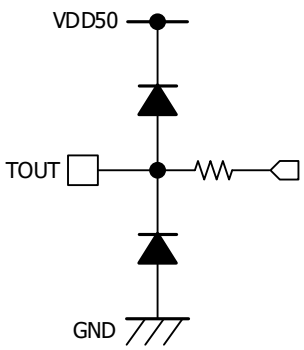
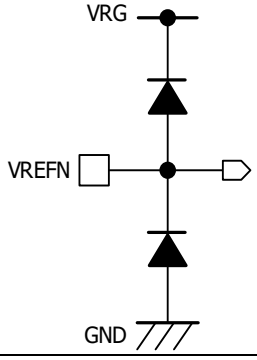
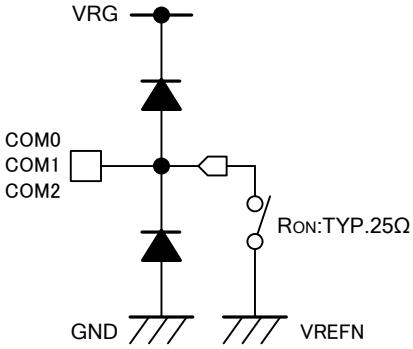
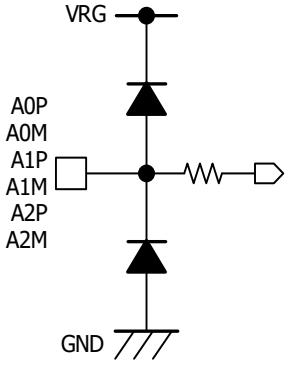
Pin name	TYPE	Equivalent circuit
RSTB	I	
TMODE0 TMODE1 EXRG	I	
GPO	O	
SCL SDA	I/O	

Table 6.4 Equivalent circuit of the pins (3/3)

Pin name	TYPE	Equivalent circuit
TOUT	O	
GND	-	—
VREFN	I	
COM0 COM1 COM2	O	
A0P A0M A1P A1M A2P A2M	I	

ABSOLUTE MAXIMUM RATINGS

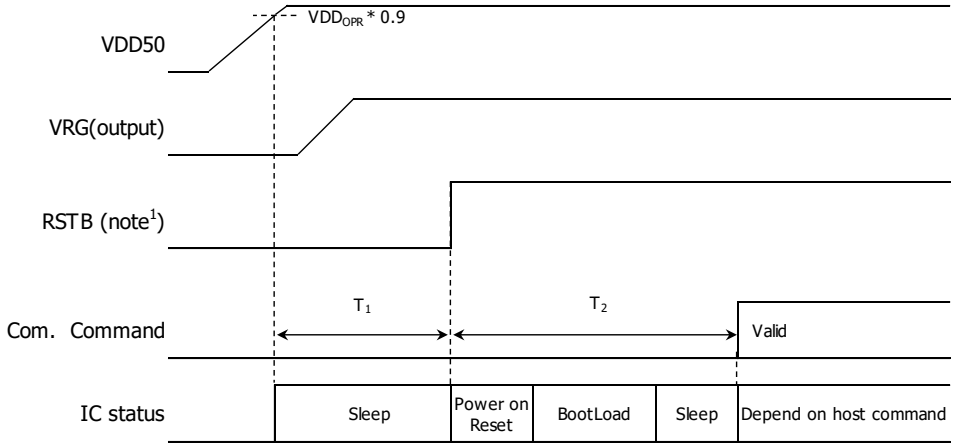
Item	Symbol	Min.	Max.	Unit
Storage temperature range	T_{STG}	-40	125	deg.C
Power supply voltage	$VDD50_{MAX}$	-0.3	6.0	V
Input voltage for VRG	VRG_{MAX}	-0.3	VDD50+0.3 (max 2.0)	V
Digital terminal voltage	$VDIG_{MAX}$	-0.3	VDD50+0.3 (max 6.0)	V
Analog terminal voltage	$VANA_{MAX}$	-0.3	VRG+0.3 (max 2.0)	V

RECOMMENDED OPERATING CONDITIONS

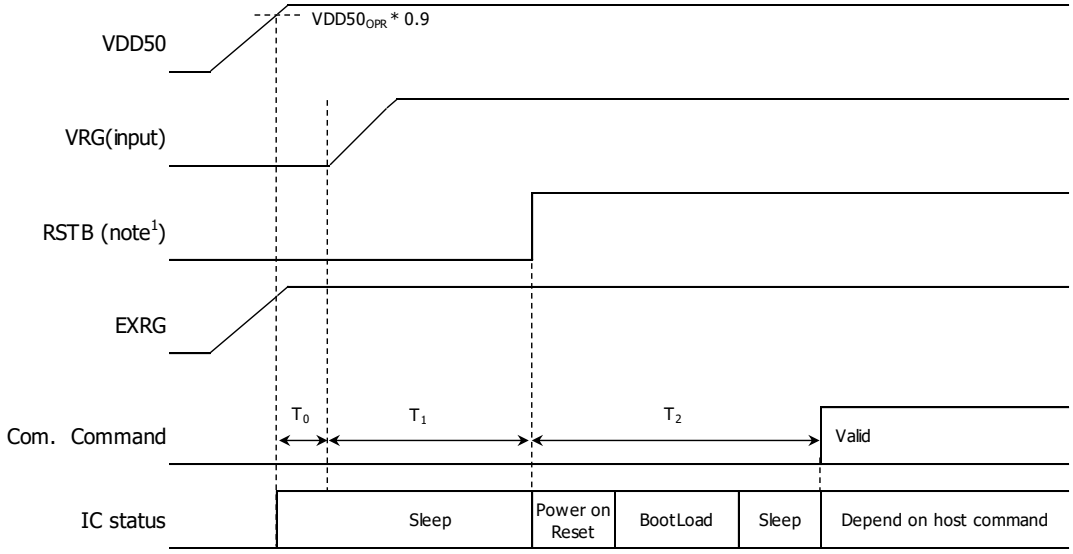
Operating temperature range, power supply voltage

Item	Symbol	Min.	Max.	Unit
Operating temperature range	T_{OPR}	-40	105	deg.C
Power supply voltage	$VDD50_{OPR}$	2.2	5.5	V
External input voltage for VRG	VRG_{OPR}	1.75	1.85	V
External input voltage for VREFP	$VREFP_{OPR}$	1.75	1.85	V
Internal regulator output current	$IVRG_{O}$	0	16	mA

・ Sequence of Power-ON (Internal regulate mode)

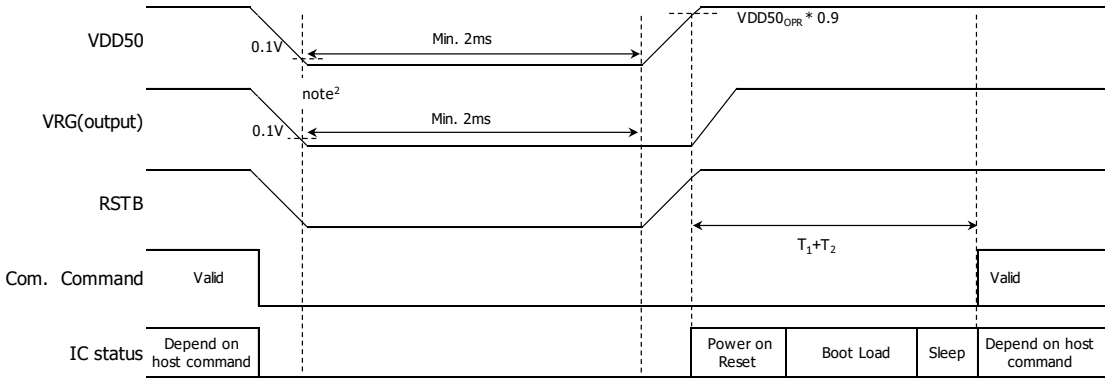


・ Sequence of Power-ON (VRG external input mode)

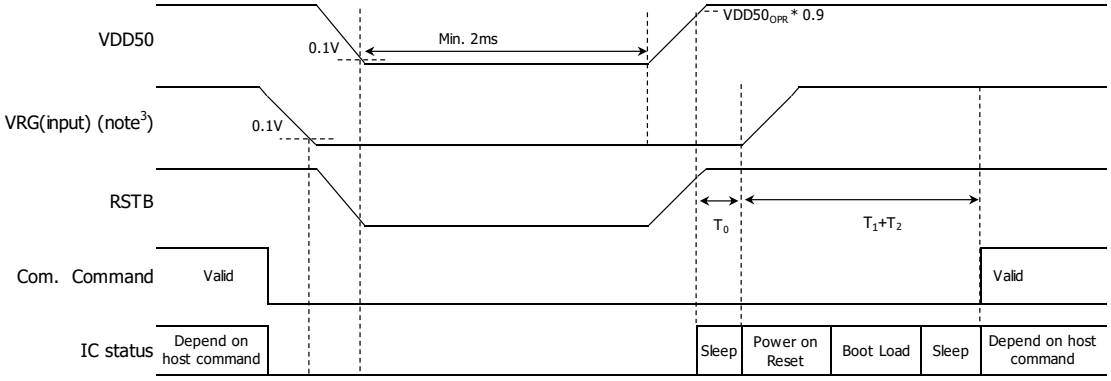


note[1]: In the figure, input Low to RSTB pin until power is turned on then input High to RSTB pin, but RSTB pin can be turned on with the open (RSTB pin is High following the power supply by internal pull-up).

・ Sequence of Power-OFF, Reboot (Internal regulate mode)



・ Sequence of Power-OFF, Reboot (VRG external input mode)



The values of waiting time T_0, T_1, T_2 at power-on are as follows. Of these, T_2 varies depending on the NVM value.

Symbol	NVM_ABh bit6 (SET_ODET) = 0		NVM_ABh bit6 (SET_ODET) = 1	
	NVM_ABh bit5 (SEL_CYC) = 0	NVM_ABh bit5 (SEL_CYC) = 1	NVM_ABh bit5 (SEL_CYC) = 0	NVM_ABh bit5 (SEL_CYC) = 1
T_0	Min. 100us			
T_1	Min. 10ms			
T_2	Min. 2ms		Min. 4ms	Min. 28.5ms

note[2]: Start at the point when at least one of VDD50 and VRG becomes 0.1 V.
(Voltage relationship between VDD50 and VRG should conform to absolute maximum ratings, recommended operating condition, note[3])

note[3]: Shut off VDD50 after shutting off VRG at VRG external input mode.

Input of sensor

Channel 0/1/2 without PGA

(unless otherwise specified, VREFP=VRG)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential input full scale range	VID_{FSR}		-VREFP	-	VREFP	V

Channel 1/2 with PGA

(unless otherwise specified, VREFP=VRG)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Common mode voltage	V_{CM}	Include variation and temperature variation	450	500	550	mV/V
Offset voltage	V_{OF}	Include variation and temperature variation	-40	-	40	mV/V
Offset voltage temperature coefficient	V_{OFTC}		-0.01	-	0.01	mV/V/deg.C
Differential input full scale range	VID_{PGA}		Refer to PGA			mV/V

ELECTRICAL CHARACTERISTICS

Current consumption

VDD50 current consumption

(unless otherwise specified, EXRG=Low (Internal regulate), Ta=-40~105deg.C, VREFP=VRG)

Item	Symbol	Condition (note[4])	Min.	Typ.	Max.	Unit
Current consumption at Sleep	I_{DDSL}	at Sleep Ta=25deg.C		1.0	3.0	uA
	I_{DDSL1}	at Sleep	-	1.0	140	
Current consumption at Standby	I_{DDSB}	at Standby Ta=25deg.C		1.2	3.2	
	I_{DDSB1}	at Standby	-	1.2	140	
VDD50 current consumption at Active	I_{DDADIT}	AD conversion of internal temperature sensor	-	0.95	1.4	mA
	$I_{DDADEX1}$	AD conversion of external sensor without amplifier (note[5])	-	0.87	1.3	
	$I_{DDADEX2}$	AD conversion of external sensor at Gain=4 to 16 (note[5])	-	4.9	5.7	
	$I_{DDADEX3}$	AD conversion of external sensor at Gain=32 to 128 (note[5])	-	5.8	6.6	

note[4]: Typ value is measured value VDD50=3.3V.
note[5]: It is not included external sensor drive current in current consumption.

VRG current consumption

(unless otherwise specified, EXRG=High(External VRG input), Ta=-40~105deg.C, VREFP=VRG)

Item	Symbol	Condition (note[6])	Min.	Typ.	Max.	Unit
VRG current consumption at Active (note[8])	I_{RGADIT}	conversion of internal temperature sensor	-	0.72	0.99	mA
	$I_{RGADEX1}$	AD conversion of external sensor without amplifier (note[7])	-	0.65	0.92	
	$I_{RGADEX2}$	AD conversion of external sensor at Gain=4 to 16 (note[7])	-	4.7	5.3	
	$I_{RGADEX3}$	AD conversion of external sensor at Gain=32 to 128 (note[7])	-	5.5	6.3	

note[6]: Typ value is measured value VDD50=3.3V and Ta=25deg.C.
note[7]: It is not included external sensor drive current in current consumption.
note[8]: This value can also be referred as the VRG current consumption in internal regulation mode.

Digital I/O

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	RSTB, TMODE0, TMODE1, EXRG, SCL, SDA	0.7 × VDD50	-	VDD50 + 0.3	V
Low level input voltage	V_{IL}	RSTB, TMODE0, TMODE1, EXRG, SCL, SDA	-0.3	-	0.3 × VDD50	V
Output voltage high-level	V_{OH}	TOUT, GPO@SEL_GPO[5:0] ≠ 00h I_{OH} = -3mA	0.8 × VDD50	-	-	V
Output voltage low-level	V_{OL1}	SCL, SDA, TOUT, GPO@SEL_GPO[5:0] ≠ 00h I_{OL} = 3mA	-	-	0.4	V
	V_{OL2}	GPO@SEL_GPO[5:0] = 00h I_{OL} = 3uA	-	-	0.4	V

Internal Regulator

(unless otherwise specified, trimmed)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VRG voltage	V_{RG}	$IVRG_O$ ≦ 110uA at Sleep, Standby	1.71	1.8	1.89	V
VRG voltage	V_{RG}	$IVRG_O$ ≦ 16mA other than Sleep, Standby	1.71	1.8	1.89	V
Output current limit	I_{LIM}	at Active	25	-	60	mA

Offset cancel circuit for external sensor

(unless otherwise specified, VREFP=VRG)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Offset voltage compensation range	V_{OF}	Channel 1, 2	-40	-	40	mV/V
Offset voltage compensation step	V_{OFST}	Channel 1, 2	-	256	-	step

PGA Programmable Gain Amplifier

(unless otherwise specified, VREFP=VRG)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Gain setting	G_V	Setting CHx_GAIN[2:0]	1	-	128	V/V
Gain setting step	G_{ST}		-	8	-	step
Gain error	G_{ERR}		-5	-	5	%

Unit : mV/V

Item	Symbol	Gain [V/V]						
		1	4	8	16	32	64	128
Differential input full scale range	VID_{PGA}	±450	±121	±59.3	±28.1	±15.6	±6.24	±1.55

PGA output voltage (ideal value) is shown in the following equation.

$$V_{OUT} = G_v * (V_{INP} - V_{INM}) = G_v * VID_{PGA}$$

*V_{INP} = PGA input voltage plus
V_{INM} = PGA input voltage minus
G_V = Gain setting
VID_{PGA} = Differential input full scale voltage

Temperature sensor

※3rd order correction
(unless otherwise specified, VREFP=VRG)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolustion	T_{RES}		-	16	-	bits
Temperature sensitivity	T_{Sens}	Ta = -40 ~ +105deg.C	1.70	-	2.77	mV/ deg.C/VREF

TYPICAL APPLICATION CIRCUIT

Input channel and target sensor

Table 10.1 Input channel and target sensor

Input channel	Temperature sensor	Physical sensor
Channel 0 (A0P, A0M, COM0)	connect OK	connect NG
Channel 1 (A1P, A1M, COM1)	connect OK	connect OK
Channel 2 (A2P, A2M, COM2)	connect OK	connect OK

Strain gauge

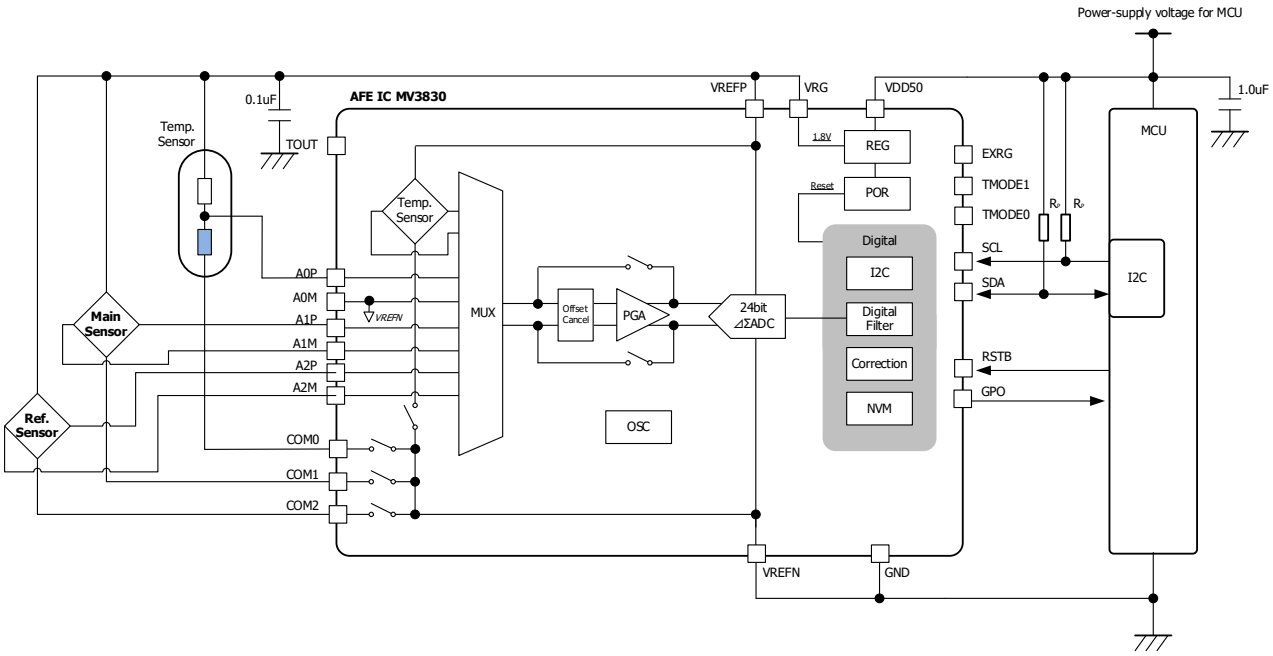


Fig. 10.1 Strain gauge

Caution about external capacitor

1) VDD50 and VRG must be connected with specified capacitors so that MV3830 can be stable.
2) For VDD50, we recommend to use a capacitor whose nominal value is 1.0uF, capacitance tolerance ±20% or less, and temperature characteristics ±22% or less.
3) For VRG, we recommend to use a capacitor whose nominal value is 1.0uF, capacitance tolerance ±10% or less, and temperature characteristics ±15% or less. If any capacitor is not connected, MV3830 may be broken.
4) If a filter is placed between the sensor outputs (A1P/A1M or A2P/A2M), we recommended to use a capacitor of 1.2nF or less. If a capacitor of 1.2nF or more is used, the open fault detection function may not work properly.

TYPICAL PERFORMANCE CHARACTERISTICS

Integral non-linearity

(unless otherwise specified, Ta=25deg.C,VREFP=VRG, note[9])

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
INL	INL	common mode voltage = VREFP/2	-	±150	-	ppm of FSR (note[10])

note[9]: average number = 1time, IIR_FILT = OFF
note[10]: FSR = 2VREF/Gain, VREF = VREFP - VREFN

ADC output code (ideal value) is shown in the following equation.

$$D_{OUT} = \frac{V_{INP} - V_{INM}}{V_{LSB}} = (V_{INP} - V_{INM}) * \frac{2^{24}}{4(VREFP - VREFN)}$$

*V_{INP} = ADC input voltage plus
V_{INM} = ADC input voltage minus
VREFP = VREFP voltage, VREFN = VREFN voltage
V_{LSB} = voltage per 1LSB

Input referred voltage noise

RMS value

CH0 (unless otherwise specified, without sensor, Ta=25deg.C, VDD50=3.3V, note[11]) Unit:uVrms

OSR	conversion time @Normal Mode	conversion time @Sequential Mode	Symbol	Gain [V/V]						
				1 note12	4	8	16	32	64	128
256	1.18ms	0.39ms	V_{nrms1}	30.95	8.19	4.48	2.85	2.30	2.14	2.10
512	2.35ms	0.78ms	V_{nrms2}	11.39	3.42	2.14	1.64	1.51	1.48	1.48
1024	4.70ms	1.56ms	V_{nrms3}	7.33	2.27	1.45	1.14	1.07	1.05	1.04
2048	9.38ms	3.13ms	V_{nrms4}	5.15	1.60	1.02	0.80	0.75	0.74	0.74

CH1, CH2 (unless otherwise specified, without sensor, Ta=25deg.C, VDD50=3.3V, note[11]) Unit:uVrms

OSR	AD conversion time @Normal Mode	AD conversion time @Sequential Mode	Symbol	Gain [V/V]						
				1 note12	4	8	16	32	64	128
256	1.18ms	0.39ms	V_{nrms1}	30.95	8.16	4.42	2.76	2.19	2.02	1.98
512	2.35ms	0.78ms	V_{nrms2}	11.39	3.38	2.08	1.56	1.43	1.40	1.39
1024	4.70ms	1.56ms	V_{nrms3}	7.33	2.24	1.41	1.08	1.01	0.99	0.98
2048	9.38ms	3.13ms	V_{nrms4}	5.15	1.58	0.99	0.76	0.71	0.70	0.70

note[11]: VREFP=VRG, average number=1time, IIR_FILT=OFF
note[12]: CHx_GAIN[2:0]=000b or 001b

Peak-to-Peak value

CH0 (unless otherwise specified, without sensor, Ta=25deg.C, VDD50=3.3V, note[13]) Unit：uV

OSR	AD conversion time @Normal Mode	AD conversion time @Sequential Mode	Symbol	Gain [V/V]						
				1 note14	4	8	16	32	64	128
256	1.18ms	0.39ms	V_{npp1}	204.3	54.05	29.57	18.81	15.18	14.12	13.86
512	2.35ms	0.78ms	V_{npp2}	75.17	22.57	14.12	10.82	9.97	9.77	9.77
1024	4.70ms	1.56ms	V_{npp3}	48.38	14.98	9.57	7.52	7.06	6.93	6.86
2048	9.38ms	3.13ms	V_{npp4}	33.99	10.56	6.73	5.28	4.95	4.88	4.88

CH1, CH2 (unless otherwise specified, without sensor, Ta=25deg.C, VDD50=3.3V, note[13]) Unit：uV

OSR	AD conversion time @Normal Mode	AD conversion time @Sequential Mode	Symbol	Gain [V/V]						
				1 note14	4	8	16	32	64	128
256	1.18ms	0.39ms	V_{npp1}	204.3	53.86	29.17	18.22	14.45	13.33	13.07
512	2.35ms	0.78ms	V_{npp2}	75.17	22.31	13.73	10.30	9.44	9.24	9.17
1024	4.70ms	1.56ms	V_{npp3}	48.38	14.78	9.31	7.13	6.67	6.53	6.47
2048	9.38ms	3.13ms	V_{npp4}	33.99	10.43	6.53	5.02	4.69	4.62	4.62

note[13]: VREFP=VRG, average number=1time, IIR_FILT=OFF
note[14]: CHx_GAIN[2:0]=000b or 001b

AD conversion time (Typical value)

Normal Mode

(unless otherwise specified, Ta=25deg.C, VDD50=3.3V, VREFP=VRG) Unit：ms

Item	Symbol	Number of averaging times	OSR			
			256	512	1024	2048
AD conversion time (Normal Mode)	$T_{nmconv1}$	1	1.18	2.35	4.70	9.38
	$T_{nmconv2}$	2	1.57	3.14	6.26	12.51
	$T_{nmconv3}$	3	1.96	3.92	7.82	15.64
	$T_{nmconv4}$	4	2.35	4.70	9.39	18.76
	$T_{nmconv5}$	5	2.75	5.48	10.95	21.89
	$T_{nmconv6}$	6	3.14	6.26	12.51	25.01
	$T_{nmconv7}$	7	3.53	7.04	14.07	28.14
	$T_{nmconv8}$	8	3.92	7.82	15.64	31.26

Sequential Mode

(unless otherwise specified, Ta=25deg.C, VDD50=3.3V, VREFP=VRG) Unit：ms

Item	Symbol	Number of averaging times	OSR			
			256	512	1024	2048
AD conversion time (Sequential Mode)	$T_{smconv1}$	1	0.39	0.78	1.56	3.13
	$T_{smconv2}$	2	0.78	1.56	3.13	6.25
	$T_{smconv3}$	3	1.17	2.34	4.69	9.38
	$T_{smconv4}$	4	1.56	3.13	6.25	12.50
	$T_{smconv5}$	5	1.95	3.91	7.81	15.63
	$T_{smconv6}$	6	2.34	4.69	9.38	18.75
	$T_{smconv7}$	7	2.73	5.47	10.94	21.88
	$T_{smconv8}$	8	3.13	6.25	12.50	25.00

After operating Sequential Mode command, it takes conversion time same as Normal Mode until taking the first conversion result. After that, it takes conversion time in the table during Sequential Mode.

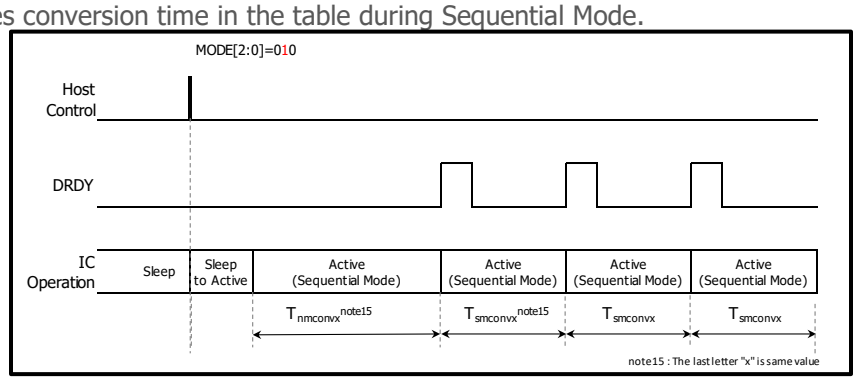


Fig. 11.1 AD conversion time (Sequential Mode)

AC characteristics

(unless otherwise specified, Ta=25deg.C, VDD50=3.3V, VREFP=VRG)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift time to Active	$T_{slp2act}$	Sleep/Standby → Active	-	0.42	1.3	ms
AD conversion interval (Normal Mode)	$T_{interval1}$	TSTBY[2:0]=000b	-	0	-	ms
	$T_{interval2}$	TSTBY[2:0]=001b	-	10	-	
	$T_{interval3}$	TSTBY[2:0]=010b	-	100	-	
	$T_{interval4}$	TSTBY[2:0]=011b	-	400	-	
	$T_{interval5}$	TSTBY[2:0] =100b, 101b, 110b	-	1000	-	
	$T_{interval6}$	TSTBY[1:0]=111b	One Shot			
DRDY pulse width	T_{drdy}	C_{OL}≦100pF	-	0.2	-	ms

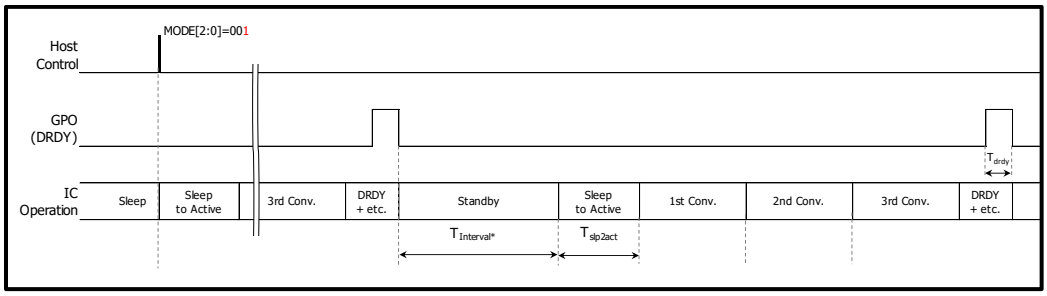
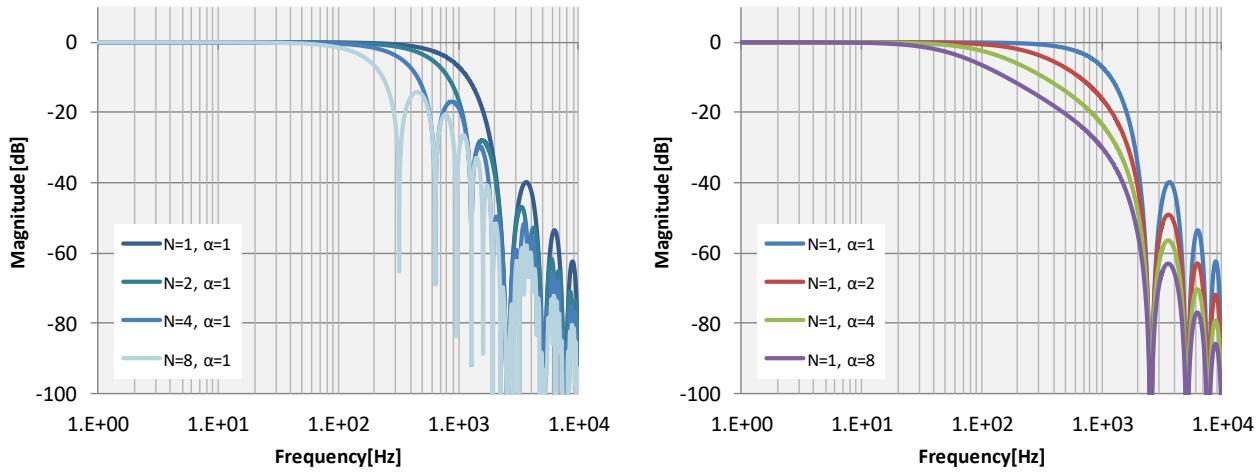


Fig. 11.2 AD conversion interval (Normal Mode)

Filter characteristics

(unless otherwise specified, Ta=25deg.C, VDD50=3.3, VREFP=VRG)

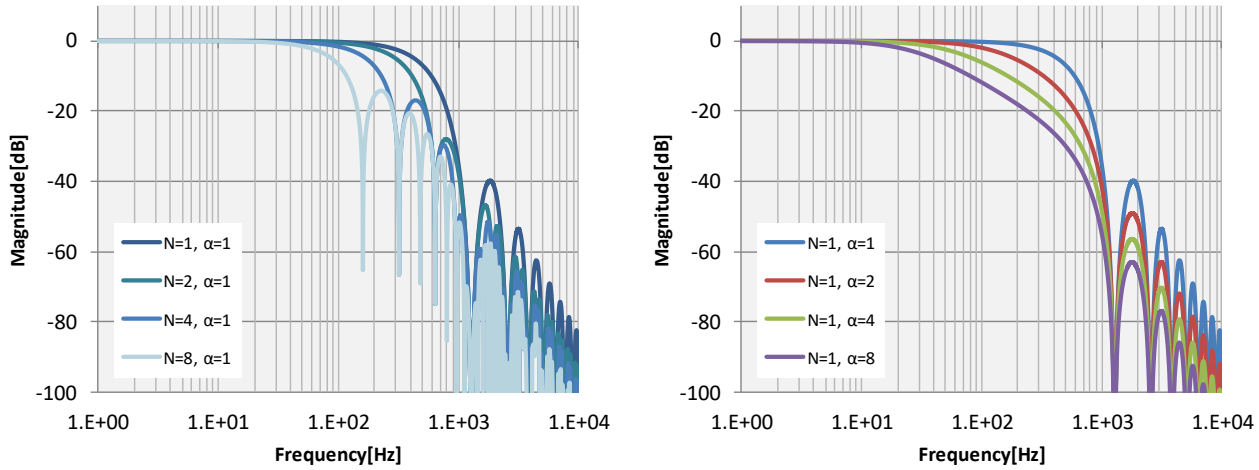
■OSR=256



(a) N_{ave} dependence at IIR coefficient = 1 (b) IIR coefficient dependence at N_{ave} = 1

Fig. 11.3 Filter characteristics at OSR=256

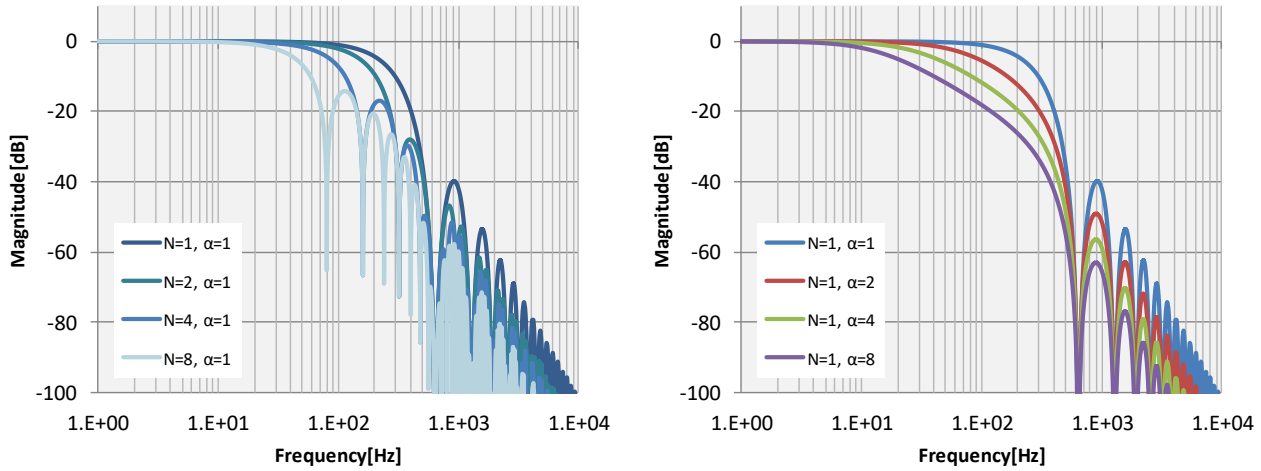
■OSR=512



(a) N_{ave} dependence at IIR coefficient = 1 (b) IIR coefficient dependence at N_{ave} = 1

Fig. 11.4 Filter characteristics at OSR=512

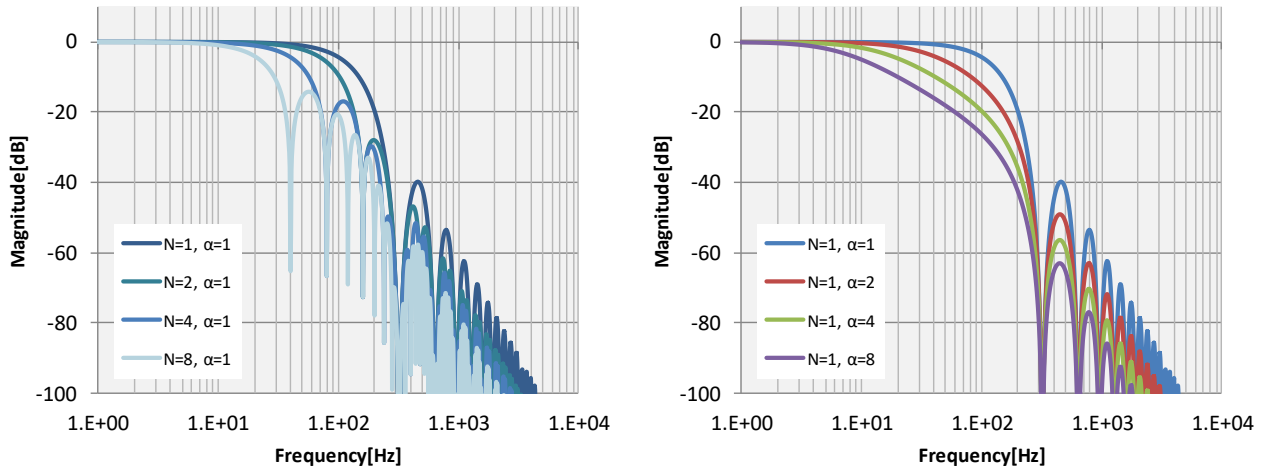
■OSR=1024



(a) N_{ave} dependence at IIR coefficient = 1 (b) IIR coefficient dependence at N_{ave} = 1

Fig. 11.5 Filter characteristics at OSR=1024

■OSR=2048



(a) N_{ave} dependence at IIR coefficient = 1 (b) IIR coefficient dependence at N_{ave} = 1

Fig. 11.6 Filter characteristics at OSR=2048

Internal regulator DC characteristics

(unless otherwise specified, Ta=25deg.C, VDD50=3.3, VREFP=VRG)

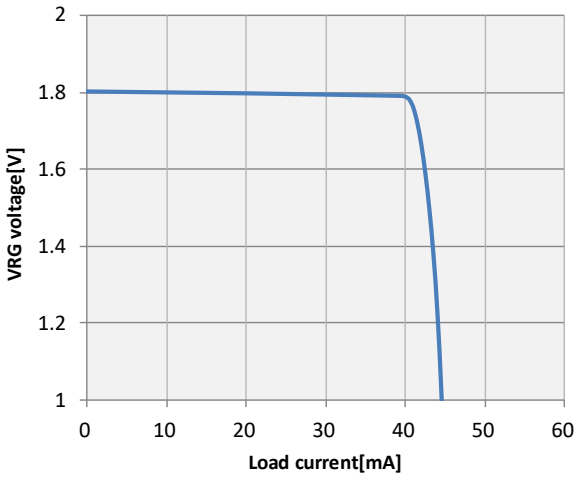


Fig. 11.7 DC load current characteristics

Current consumption at Sleep

(unless otherwise specified, VDD50=3.3, VREFP=VRG)

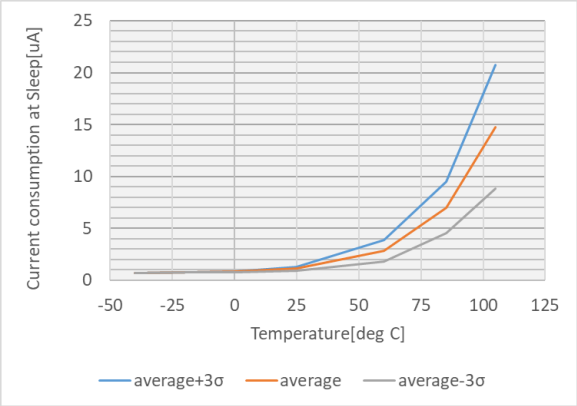


Fig. 11.8 Current consumption at Sleep

Current consumption at Standby

(unless otherwise specified, VDD50=3.3, VREFP=VRG)

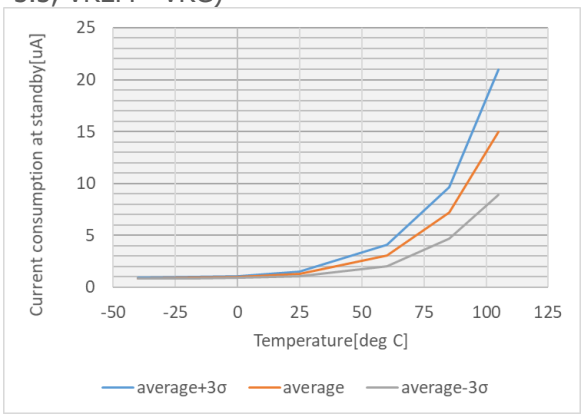


Fig. 11.9 Current consumption at Standby

Temperature sensor

(unless otherwise specified, VDD50=3.3, VREFP=VRG)

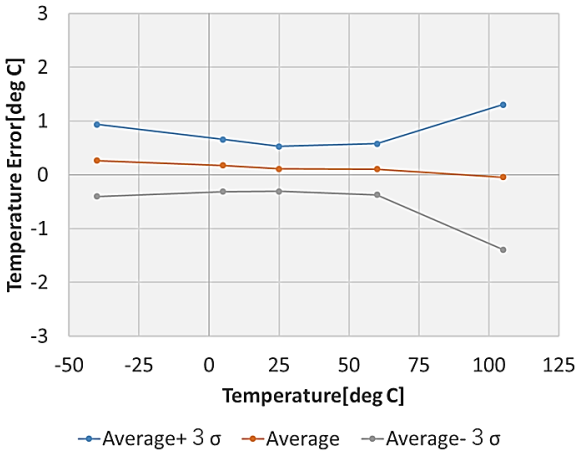


Fig. 11.10 Temperature error of internal temperature sensor

Temperature error when using the correction coefficient written in NVM at the time of shipment.
If adjusted by the user, it follows the accuracy of the adjustment system.

OPERATION DESCRIPTION

Overview

The overview of MV3830 operation is shown below.

■The mode to reduce current consumption at Active

1) Sleep Mode: Only to receive command. Unable to access NVM.

■The mode for AD conversion

1) Normal Mod: After receiving start command, MV3830 continuously or single measures by setting AD conversion time. Target sensor is from one to three.
2) Sequential Mode: After receiving start command, MV3830 continuously measures. Target sensor is only one.

The flow from Power-ON to AD conversion is shown below.

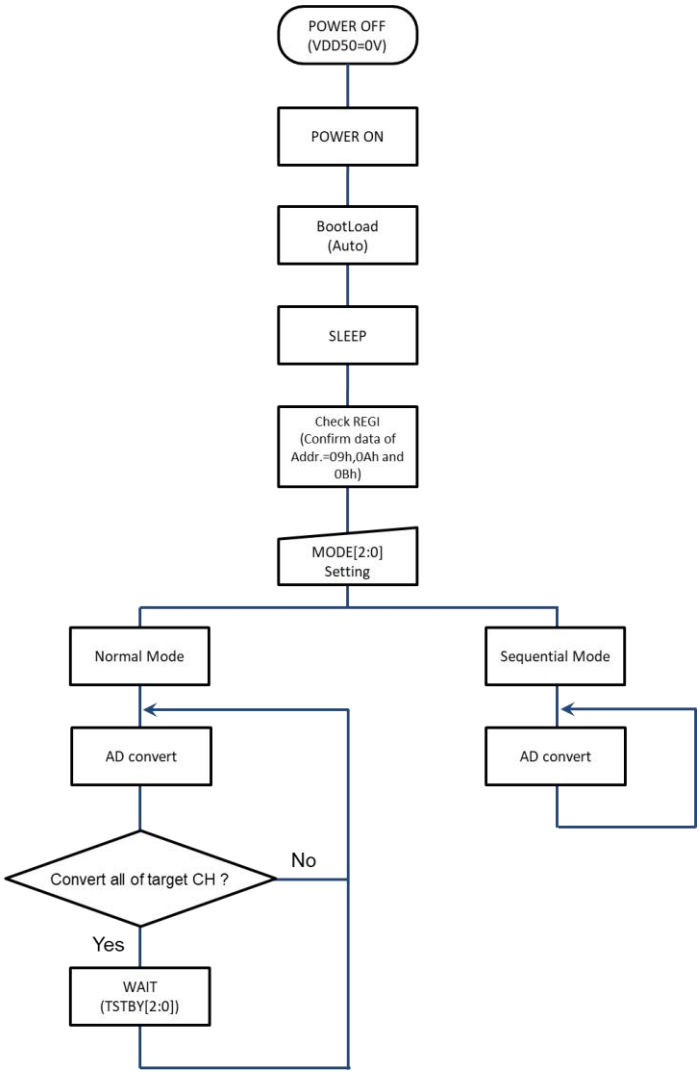


Fig. 12.1 Flow from Power-ON to AD conversion

Normal Mode

The IC continuously measures for 1 to 3 sensors in this mode. And it can be set the interval of continuous measurement.

Table 12.1 Register for Normal Mode setting

Addr.		Bit	Default	Description
Value	Name			
0Fh	MEAS_CTRL	TSTBY[2:0]	00h	Setting for AD conversion interval
		MODE[2:0]		Operation setting
0Eh	MEAS_EN	EN_1ST[1:0]	00h	Setting for 1st measurement target
		EN_2ND[1:0]		Setting for 2nd measurement target
		EN_3RD[1:0]		Setting for 3rd measurement target

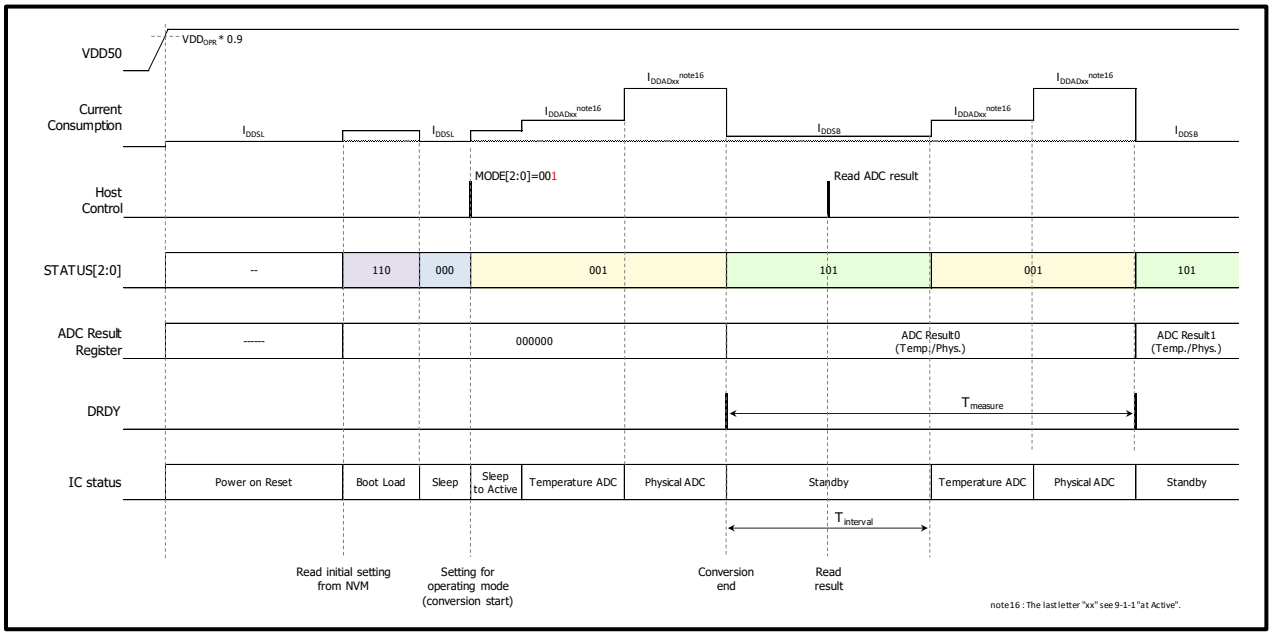


Fig. 12.2 Normal Mode timing

DRDY (B) is a signal notifying completion of AD conversion data preparation. Execute data acquisition command at DRDY (B) change timing when acquire data in sync with AD conversion. DRDY (B) output timing may change When communication including I2C is performed. DRDY (B) at Normal Mode output timing is delayed When I2C and MV3830 transfer timing conflicts.

Sequential Mode

The IC continuously measures for one sensor in this operating mode.

Table 12.2 Register for Sequential Mode setting

Addr.		Bit	Default	Description
Value	Name			
0Fh	MEAS_CTRL	MODE[2:0]	00h	Operation Setting
0Eh	MEAS_EN	SET_SEQ[1:0]	00h	Setting for measurement target

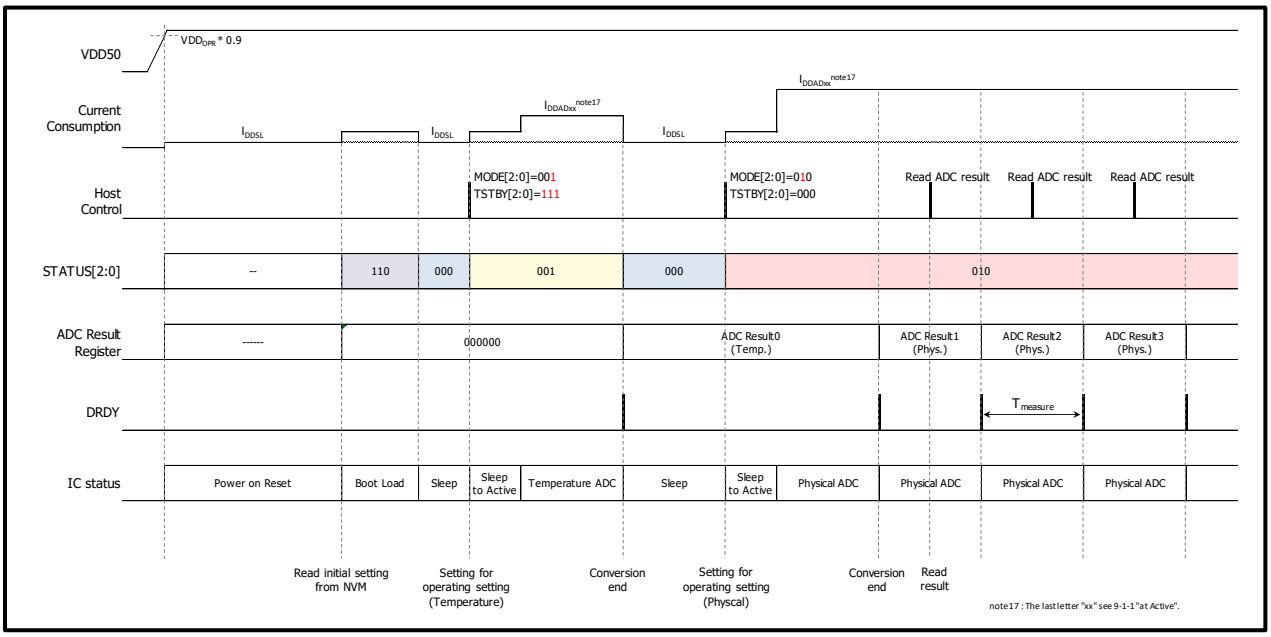


Fig. 12.3 Sequential Mode timing

It differs from Normal Mode in the following points. DRDY (B) output timing of Sequential Mode does not change, and the data is sent at the communication start timing When I2C and MV3830 transfer timing conflicts.

Correction operation

By executing the mode for AD conversion, a correction operation is automatically performed for each AD conversion using the correction coefficient previously written in the NVM, and the AD conversion result subjected to the secondary (or tertiary) correction can be retrieved. Please refer to the application note for correction coefficient calculation. Here, only the correction formula using the correction coefficient is shown.

Temperature sensor

The formula of correction calculation for temperature sensor is shown below.

$$AD_{correct} = \left\{\left(\frac{CC\_TSENS\_T \times 2^8 \times AD_{raw}}{2^{24-2\times BS\_TSENS\_T}} + CC\_TSENS\_S \times 2^8\right) \times \frac{AD_{raw}}{2^{24-2\times BS\_TSENS\_S}} + CC\_TSENS\_F \times 2^8\right\} \times \frac{AD_{raw}}{2^{24-2\times BS\_TSENS\_F}} + CC\_TSENS\_Z \times 2^8$$

Symbol	Register Name	Contents	Bit	Register	NVM
CC_TSENS_T	CC_CH0_T/ CC_CH1_FZ/ CC_CH2_FZ	3rd order correction coefficient	16	18h-19h/ 20h-21h/ 38h-39h	86h/ 8Ah/ 96h
CC_TSENS_S	CC_CH0_S/ CC_CH1_ZS/ CC_CH2_ZS	2nd order correction coefficient	16	16h-17h/ 1Eh-1Fh/ 36h-37h	85h/ 89h/ 95h
CC_TSENS_F	CC_CH0_F/ CC_CH1_ZF/ CC_CH2_ZF	1st order correction coefficient	16	14h-15h/ 1Ch-1Dh/ 34h-35h	84h/ 88h/ 94h
CC_TSENS_Z	CC_CH0_Z/ CC_CH1_ZZ/ CC_CH2_ZZ	Zero order correction coefficient	16	12h-13h/ 1Ah-1Bh/ 32h-33h	83h/ 87h/ 93h
BS_TSENS_T	BITSHIFT_CH0_T/ BITSHIFT_CH1_FF/ BITSHIFT_CH2_FF	Bit shift of A_T	4	4Bh_B[7:4]/ 4Ch_B[3:0]/ 52h_B[3:0]	9Fh_B[7:4]/ A0h_B[11:8]/ A3h_B[11:8]
BS_TSENS_S	BITSHIFT_CH0_S/ BITSHIFT_CH1_ZS/ BITSHIFT_CH2_ZS	Bit shift of B_T	4	4Ah_B[3:0]/ 4Ch_B[7:4]/ 52h_B[7:4]	9Fh_B[11:8]/ A0h_B[15:12]/ A3h_B[15:12]
BS_TSENS_F	BITSHIFT_CH0_F/ BITSHIFT_CH1_ZF/ BITSHIFT_CH2_ZF	Bit shift of C_T	4	4Ah_B[7:4]/ 4Bh_B[3:0]/ 51h_B[3:0]	9Fh_B[15:12]/ 9Fh_B[3:0]/ A2h_B[3:0]

$AD_{correct}$: Correction value of temperature sensor
AD_{raw} : AD raw data of temperature sensor

※register value is 2's complement

Physical sensor (resistive bridge type)

The formula of correction calculation for physical sensor is shown below.

$$AD_{correct} = \left\{\left(\frac{phys\_3rdsens \times AD_{raw}}{2^{24-2\times BS\_PHY\_T}} + phys\_2ndsens\right) \times \frac{AD_{raw}}{2^{24-2\times BS\_PHY\_S}} + phys\_1stsens\right\} \times \frac{AD_{raw}}{2^{24-2\times BS\_PHY\_F}} + phys\_offset$$

However,

$$phys\_3rdsens = \left(\frac{CC\_PHY\_TS \times 2^8 \times AD_{temp}}{2^{24-2\times BS\_PHY\_TS}} + CC\_PHY\_TF \times 2^8\right) \times \frac{AD_{temp}}{2^{24-2\times BS\_PHY\_TF}} + CC\_PHY\_TZ \times 2^8$$

$$phys\_2ndsens = \left(\frac{CC\_PHY\_SS \times 2^8 \times AD_{temp}}{2^{24-2\times BS\_PHY\_SS}} + CC\_PHY\_SF \times 2^8\right) \times \frac{AD_{temp}}{2^{24-2\times BS\_PHY\_SF}} + CC\_PHY\_SZ \times 2^8$$

$AD_{correct}$: Correction value of physical sensor

AD_{raw} : AD raw data of physical sensor

$$phys\_offset = \left(\frac{CC\_PHY\_ZS \times 2^8 \times AD_{temp}}{2^{24-2\times BS\_PHY\_ZS}} + CC\_PHY\_ZF \times 2^8\right) \times \frac{AD_{temp}}{2^{24-2\times BS\_PHY\_ZF}} + CC\_PHY\_ZZ \times 2^8$$

Symbol	Register Name	Contents	Bit	Register	NVM
CC_PHY_TS	CC_CH1_TS/ CC_CH2_TS	2nd order coefficient for temperature	16	30h-31h/ 48h-49h	92h/ 9Eh
CC_PHY_TF	CC_CH1_TF/ CC_CH2_TF	1st order coefficient for temperature	16	2Eh-2Fh/ 46h-47h	91h/ 9Dh
CC_PHY_TZ	CC_CH1_TZ/ CC_CH2_TZ	Zero order coefficient for temperature	16	2Ch-2Dh/ 44h-45h	90h/ 9Ch
CC_PHY_SS	CC_CH1_SS/ CC_CH2_SS	2nd order coefficient for temperature	16	2Ah-2Bh/ 42h-43h	8Fh/ 9Bh
CC_PHY_SF	CC_CH1_SF/ CC_CH2_SF	1st order coefficient for temperature	16	28h-29h/ 40h-41h	8Eh/ 9Ah
CC_PHY_SZ	CC_CH1_SZ/ CC_CH2_SZ	Zero order coefficient for temperature	16	26h-27h/ 3Eh-3Fh	8Dh/ 99h
CC_PHY_FS	CC_CH1_FS/ CC_CH2_FS	2nd order coefficient for temperature	16	22h-23h/ 3Ch-3Dh	8Ch/ 98h
CC_PHY_FF	CC_CH1_FF/ CC_CH2_FF	1st order coefficient for temperature	16	20h-21h/ 3Ah-3Bh	8Bh/ 97h
CC_PHY_FZ	CC_CH1_FZ/ CC_CH2_FZ	Zero order coefficient for temperature	16	20h-21h/ 38h-39h	8Ah/ 96h
CC_PHY_ZS	CC_CH1_ZS/ CC_CH2_ZS	2nd order coefficient for temperature	16	1Eh-1Fh/ 36h-37h	89h/ 95h
CC_PHY_ZF	CC_CH1_ZF/ CC_CH2_ZF	1st order coefficient for temperature	16	1Ch-1Dh/ 34h-35h	88h/ 94h
CC_PHY_ZZ	CC_CH1_ZZ/ CC_CH2_ZZ	Zero order coefficient for temperature	16	1Ah-1Bh/ 32h-33h	87h/ 93h
BS_PHYS_T	BITSHIFT_CH1_T/ BITSHIFT_CH2_T	Bit shift	4	50h_B[3:0]/ 56h_B[3:0]	A2h_B[11:8]/ A5h_B[11:8]
BS_PHYS_S	BITSHIFT_CH1_S/ BITSHIFT_CH2_S	Bit shift	4	4Fh_B[7:4]/ 55h_B[7:4]	A1h_B[7:4]/ A4h_B[7:4]
BS_PHYS_F	BITSHIFT_CH1_F/ BITSHIFT_CH2_F	Bit shift	4	4Dh_B[3:0]/ 53h_B[3:0]	A0h_B[3:0]/ A3h_B[3:0]
BS_PHYS_TS	BITSHIFT_CH1_TS/ BITSHIFT_CH2_TS	Bit shift	4	50h_B[7:4]/ 56h_B[7:4]	A2h_B[15:12]/ A5h_B[15:12]
BS_PHYS_TF	BITSHIFT_CH1_TF/ BITSHIFT_CH2_TF	Bit shift	4	4Fh_B[3:0]/ 55h_B[3:0]	A1h_B[3:0]/ A4h_B[3:0]
BS_PHYS_SS	BITSHIFT_CH1_SS/ BITSHIFT_CH2_SS	Bit shift	4	4Eh_B[3:0]/ 54h_B[3:0]	A1h_B[11:8]/ A4h_B[11:8]
BS_PHYS_SF	BITSHIFT_CH1_SF/ BITSHIFT_CH2_SF	Bit shift	4	4Eh_B[7:4]/ 54h_B[7:4]/	A1h_B[15:12]/ A4h_B[15:12]
BS_PHYS_FS	BITSHIFT_CH1_FS/ BITSHIFT_CH2_FS	Bit shift	4	4Dh_B[7:4]/ 53h_B[7:4]	A0h_B[7:4]/ A3h_B[7:4]
BS_PHYS_FF	BITSHIFT_CH1_FF/ BITSHIFT_CH2_FF	Bit shift	4	4Ch_B[3:0]/ 52h_B[3:0]	A0h_B[11:8]/ A3h_B[11:8]
BS_PHYS_ZS	BITSHIFT_CH1_ZS/ BITSHIFT_CH2_ZS	Bit shift	4	4Ch_B[7:4]/ 52h_B[7:4]	A0h_B[15:12]/ A3h_B[15:12]
BS_PHYS_ZF	BITSHIFT_CH1_ZF/ BITSHIFT_CH2_ZF	Bit shift	4	4Bh_B[3:0]/ 51h_B[3:0]	9Fh_B[3:0]/ A2h_B[3:0

$$phys\_1stsens = \left(\frac{CC\_PHY\_FS \times 2^8 \times AD_{temp}}{2^{24-2\times BS\_PHY\_FS}} + CC\_PHY\_FF \times 2^8\right) \times \frac{AD_{temp}}{2^{24-2\times BS\_PHY\_FF}} + CC\_PHY\_FZ \times 2^8$$

T: 24bits correction temperature value

※register value is 2's complement

Retrieve temperature and physical value

The Result Register value retrieved in the mode for AD conversion is the corrected value by default. Since the correction calculation is performed automatically every AD conversion, the user can acquire temperature and physical value using the following calculation formula.
The AD result value in the temperature calculation formula assumes the AD conversion result of the temperature sensor read in 16 bits length using the RESULT READ command explained in I2C command format. When the AD conversion result of the temperature sensor is read with a length of 24 bits, substitute the value obtained by shifting the AD conversion result to the right by 8 bits into the AD result value in the formula.

Temperature (16bits output) = (AD result value - 2^{15}) / $2^{G\_TSENS\_Z}$
Pressure (24bits output) = (AD result value - 2^{23}) / $2^{G\_PHYS\_ZZ+8}$

You can substitute as below by bit operation.

Temperature (16bits output) = (MSB inversion of AD result value) / $2^{G\_TSENS\_Z}$
Pressure (24bits output) = (MSB inversion of AD result value) / $2^{G\_PHYS\_ZZ+8}$

G_TSENS_Z and G_PHYS_ZZ in the equation is the bit shift amount when programing the correction coefficient in NVM.

■Example

You can calculate temperature(16bits output) at AD result value(decimal)=5000+2^{15}、G_TSENS_Z=7
（Temperature resolution = 1 / 2^7 = 0.0078deg.C）

Temperature (16bit output) = (AD result value - 2^{15}) / $2^{G\_TSENS\_Z}$
= (5000 + 2^{15} - 2^{15}) / 2^7
= 5000 / 128
= 39.0625 [deg.C]

VRG external input mode

A part of MV3830 mounted circuit (PGA, ADC, OSC, Digital, etc.) operates with a 1.8 V power supply (VRG terminal) supplied from the built-in regulator, but the EXRG terminal to "High", it is possible to apply a 1.8 V power supply from the outside.

Time-dependent change correction function

MV3830 uses external reference sensor to correct time-dependent change. For details of them, see Register map.

Sensor open/short detector

MV3830 has Sensor open/short detector functions. MV3830 can be detected as follows when a failure occurs in the sensor connection.

■Target node

1) Sensor plus input (IC connect VREFP terminal)
2) Sensor minus input (IC connect COMx terminal, x=0,1,2)
3) Sensor plus output (IC connect AxP terminal, x=0,1,2)
4) Sensor minus output (IC connect AxM terminal, x=0,1,2)

■Failure mode

1) GND short failure: MV3830 can detect failure when host and this IC cannot communicate.
   MV3830 can detect failure when Sensor conversion value is abnormal.
2) Power line short failure: MV3830 can detect failure when Sensor conversion value is abnormal.
3) Open failure: MV3830 can detect failure when check result stack register.

■Operate of ODET

Target node detect open failure (hereinafter, this is called "sensor connection detection"). This function enables SET_ODET=1, executed BootLoad. For details of them, see Register map.

SERIAL INTERFACE

I2C Fast mode (fmax = 400kHz) of serial communication interface are supported.

Communication speed

(unless otherwise specified, Input filter=ON, $C_{OL} \leqq 400pF$)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
I2C communication speed	BR_{I2CFm}		-	-	400k	bps

I2C command format

I2C address is the total of 8 bits; the first 7 bits are slave address and the remaining 1 bit is R/W bit. Users can set the slave address (7 bits) of MV3830 optionally by writing to NVM (Default value is 0x4D). However, 0000xxx and 1111xxx cannot be used because they are reserved addresses. *Please use this product after confirming I2C specification and understanding the details.

I2C basic command format

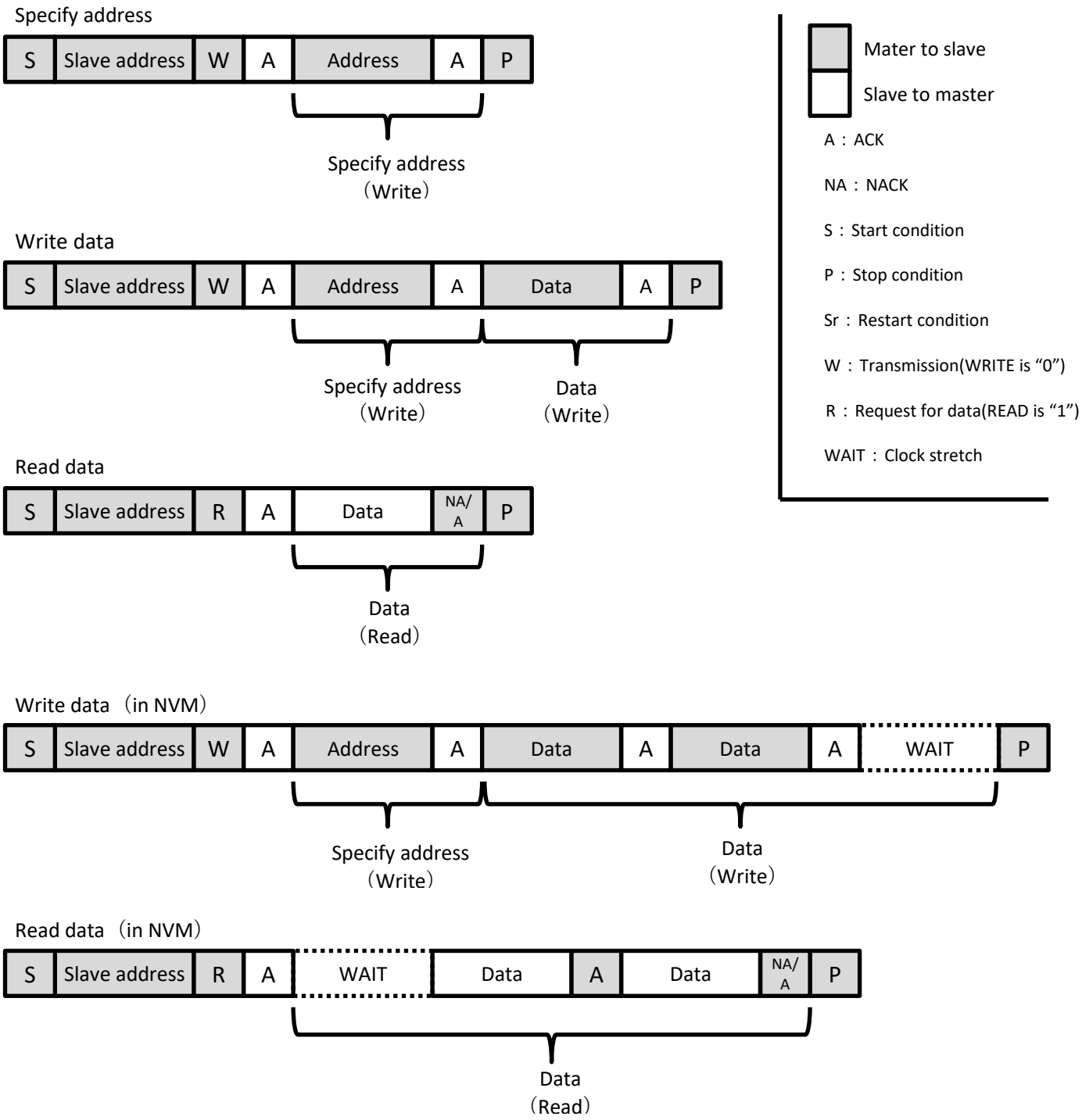


Fig. 13.1 I2C basic command format

Read only resister response

Resister of NVM set access restrictions individually. See Register address map, NVM Address map. Writing address, data of Read only resister is ACK response. No write to register because read only.

Read response on access restrictions (NACK response).

In the following case, returns NACK response when an address is specified but address itself is valid. Whether it is read/write possible depends on the access restrictions.

- Resister read can't access by access restrictions.
- NVM read by state of BootLoad and ACTIVE (independent of access level).
- Reading unmapped areas.

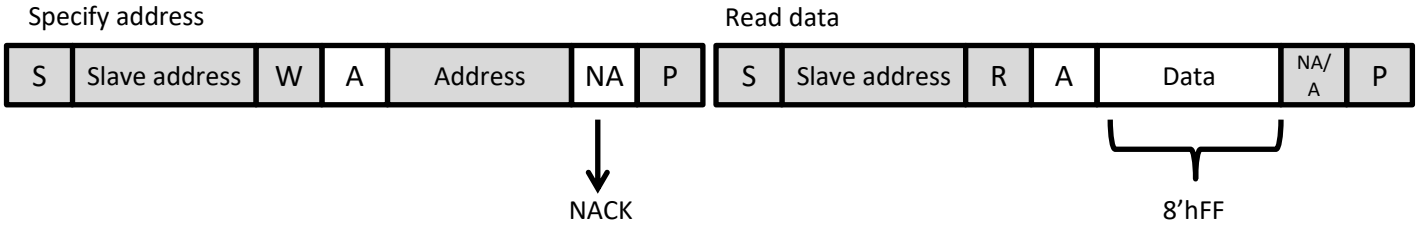


Fig. 13.2 Read response on access restrictions

RESULT READ command format

With RESULT READ command, MV3830 reads the data without address designation to transfer the status and the data of RES_STACK1, RES_STACK2, and RES_STACK3, which are stored in the register address 8'h00 to 8'h08, in sequence to the host. However, it the response when writing the address immediately before this command must be an ACK response.

After the master receives 1-byte data and returns ACK, the next 1-byte data is sent to the master. If it returns NACK, the data sent subsequently will be 8'hFF. The readable data value of the IC changes by error detection setting (SET_CRC setting) of I2C communication. The read data value is shown below.

With CRC (SET_CRC=0), when the master reads the data exceeding 9 bytes, the data of 10 bytes and after will be 8'hFF. Without CRC (SET_CRC=1), when the master reads the data exceeding 12 bytes, the data of 13 bytes and after will be 8'hFF.

The data length is set for each channel, and it is 16 or 24 bits from the top of the AD conversion result. Status grant and data length are set following register address 8'h57.

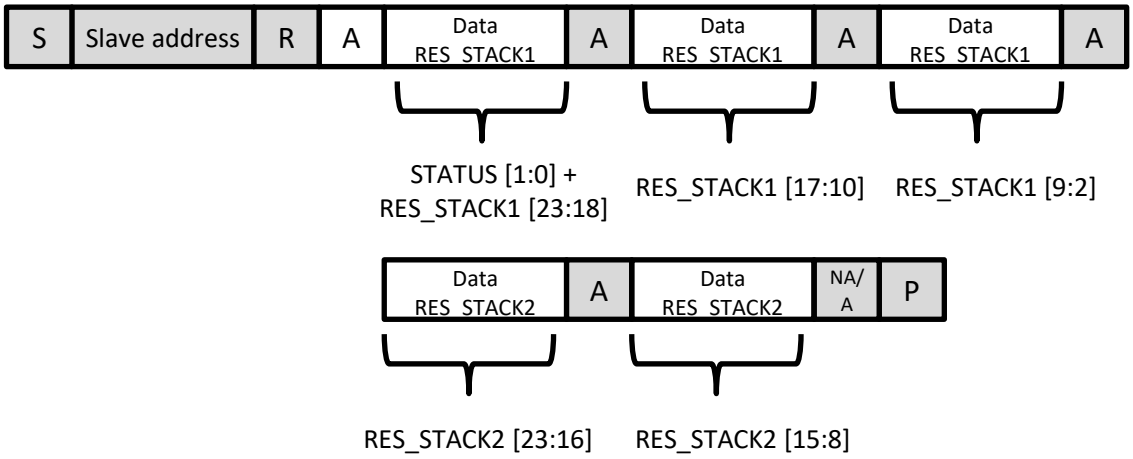


Fig. 13.3 RESULT READ command format with status

READ command format

With READ command, MV3830 reads the data after address designation to transfer it. To read the data from NVM region, it performs clock stretching before reading.

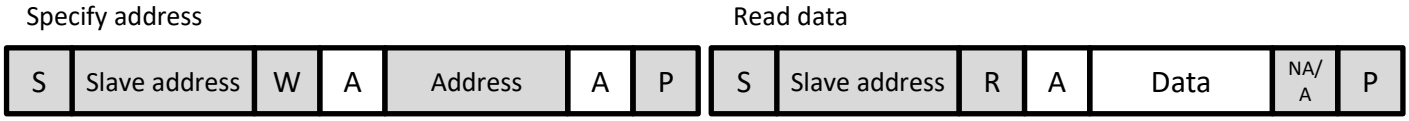


Fig. 13.4 READ command format

WRITE command format

With WRITE command, MV3830 sends the write data after address designation to write values. To write the data in NVM region, it performs clock stretching after the master receives ACK for the write data.

Fig. 13.5 WRITE command format

BURST READ command format

With BURST READ command, a process that ACK is returned after 1-byte data is transferred is repeated. When NACK is returned, the subsequent processing is terminated and 8'hFF data is transferred.
Addresses are automatically incremented. When a register address reaches 8'h7F and 8'hAF, it is no longer incremented and the processing is repeated at the same address.

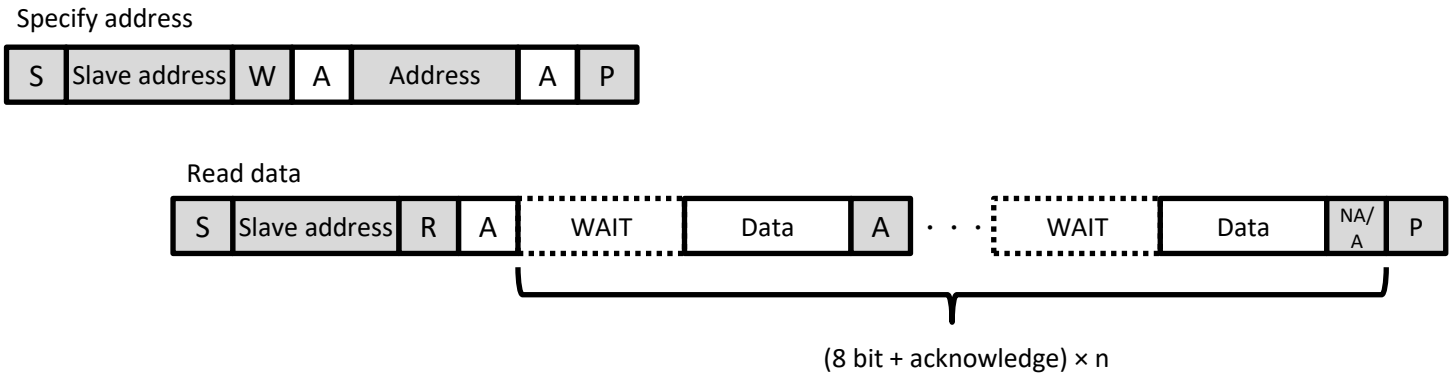


Fig. 13.6 BURST READ command format

BURST WRITE command format

With BURST WRITE command, 1-byte data is repeatedly written.
Addresses are automatically incremented. When a register address reaches 8'h7F and 8'hAF, it is no longer incremented and the processing is repeated at the same address.

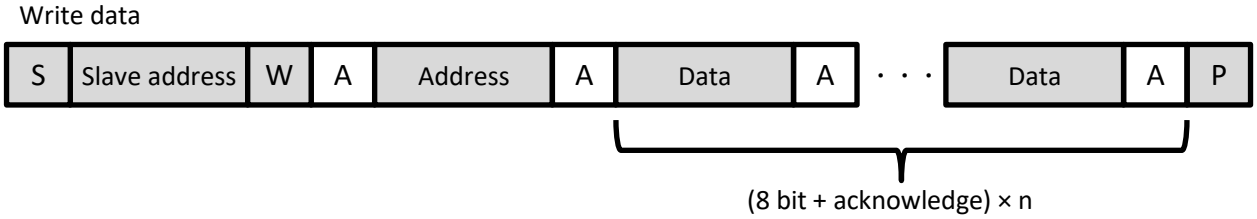


Fig. 13.7 BURST WRITE command format

Restart condition

The communication continues using Restart condition instead of the combination of start condition and stop condition as a condition between address designation and data read.

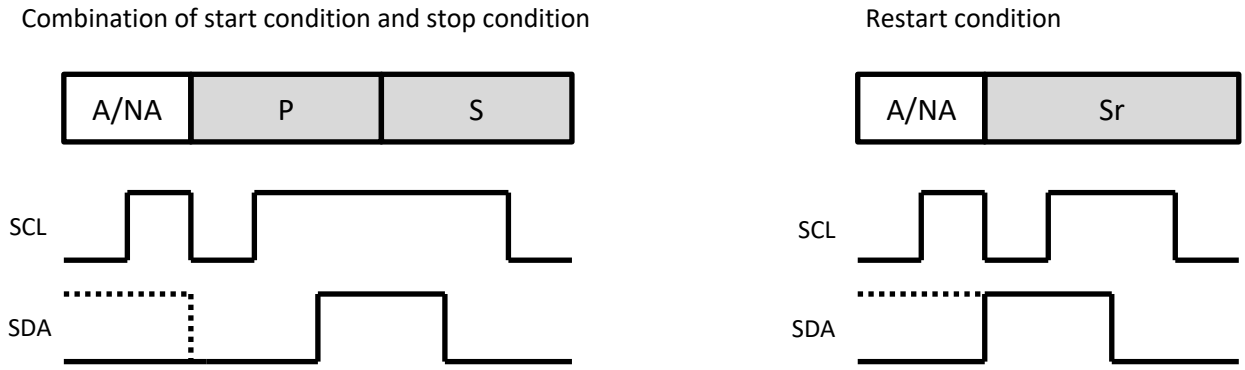


Fig. 13.8 Restart condition

CRC addition function for error detection of I2C

MV3830 has a CRC addition function to detect accidental data error of I2C communication. This function becomes valid by setting SET_CRC=1 of register FILT_SET. The specification is shown below.

Table 13.1 CRC addition function for error detection of I2C communication

Item	Description
Condition	SET_CRC=1
Check target	All register（Addr.=00h～66h）
Command	READ, BURST READ, RESULT READ
Name	CRC-8-Dallas/Maxim
Polynomial	$x^8 + x^5 + x^4 + 1$
Initial value	8'hFF
Clear condition	clear every CRC output
Output inversion	no
CRC value of registers under access control	8'hFF

READ command

CRC value is calculated from Slave address+R, Address and Data.

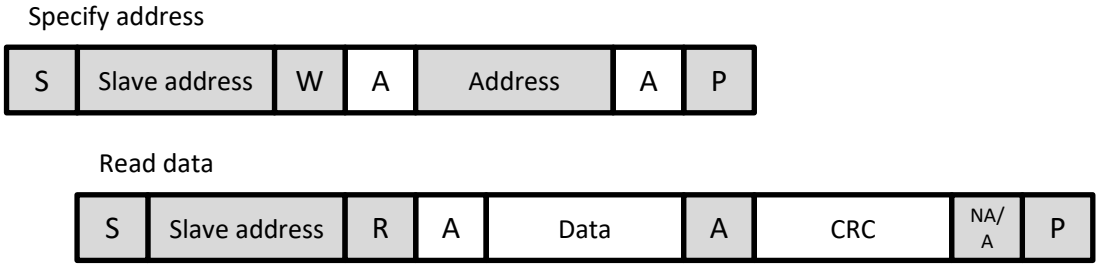


Fig. 13.9 READ + CRC command format

BURST READ command

First CRC value is calculated from Slave address+R, Address and Data.
Next CRC value is calculated from only Data.

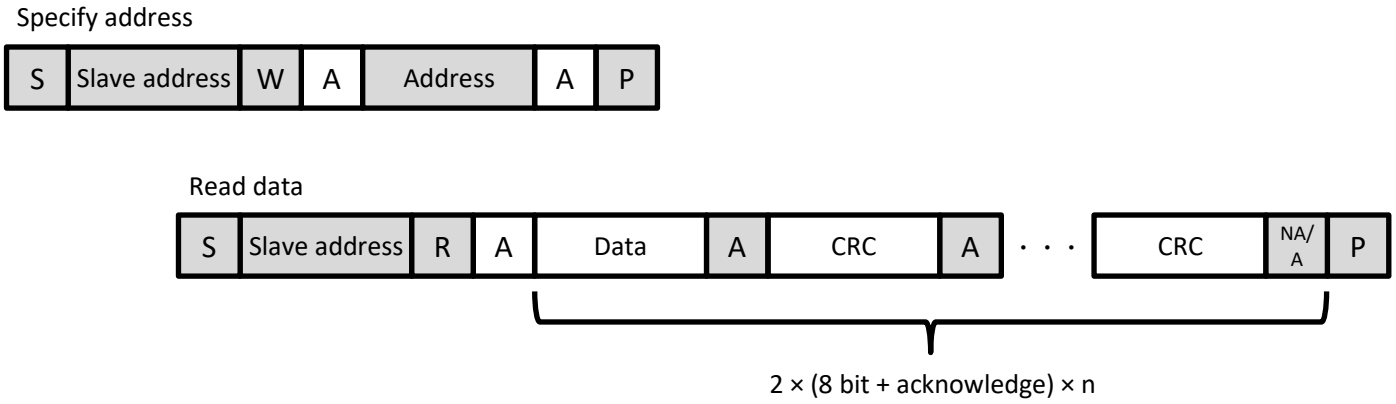


Fig. 13.10 BURST READ + CRC command format

RESULT READ command

First CRC value is calculated from Slave address +R, STATUS and RES_STACK1.
Next CRC value is calculated from RES_STACK2.
For details of STATUS, refer to the description of register address 8'h57.

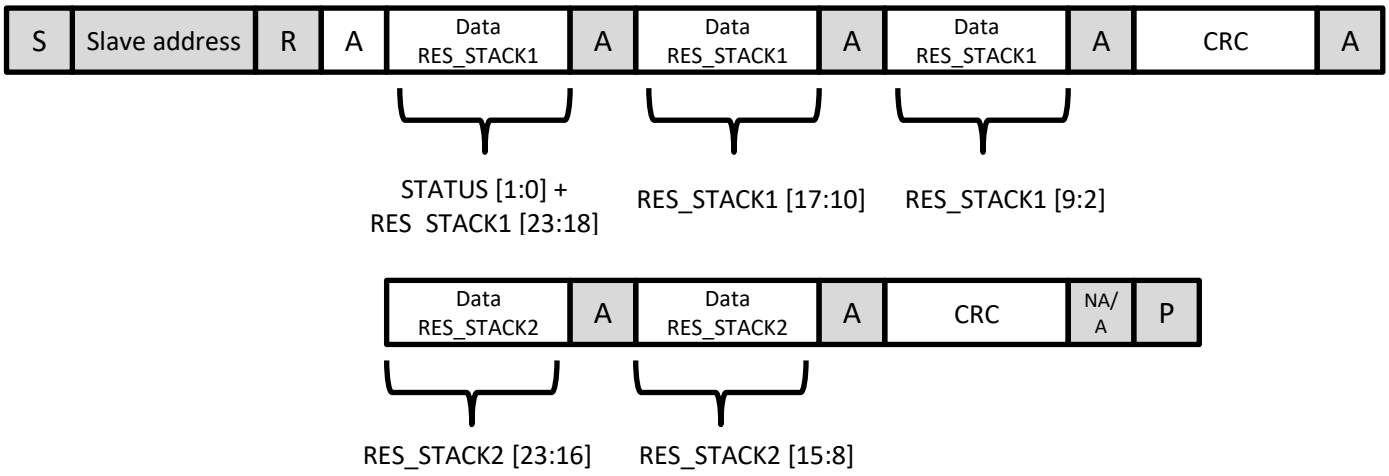


Fig. 13.11 RESULT READ + CRC command format

I2C AC characteristics

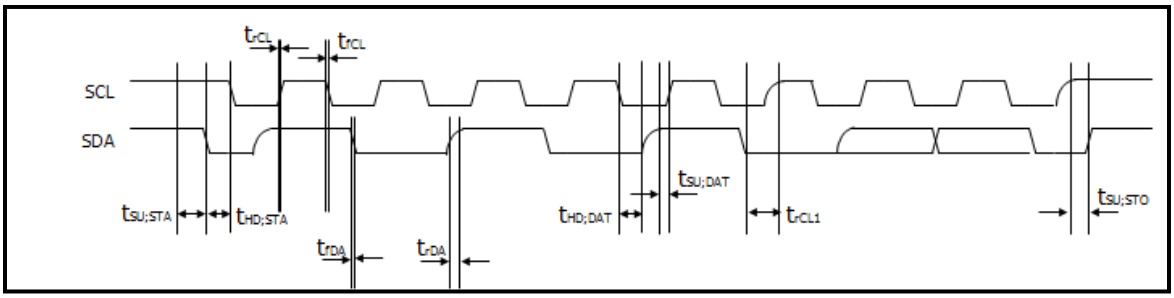


Fig. 13.12 I2C AC timing

(unless otherwise specified, Input filter=ON, $C_{OL} \leqq 400pF$)

Item	Symbol	Fast mode			Unit
		min.	typ.	max.	
SCL clock frequency	f_{SCL}	0	-	400k	Hz
Start condition setup time	$t_{SU;STA}$	600	-	-	ns
Start condition hold time	$t_{HD;STA}$	600	-	-	ns
Stop condition setup time	$t_{SU;STO}$	600	-	-	ns
Data setup time	$t_{SU;DAT}$	100	-	-	ns
Data hold time (note[17])	$t_{HD;DAT}$	20	-	-	ns
SCL rise time	t_{rCL}	-	-	300	ns
SCL fall time	t_{fCL}	10	-	300	ns
SDA rise time	t_{rDA}	-	-	300	ns
SDA fall time	t_{fDA}	10	-	300	ns

note[17]: This product does not have the function to retain data in SDA. Please ensure the hold of SDA with 20nsec for the area where SCL falling edge is not defined.

STATE

State definition

State definition is shown below.

1) Sleep : Able to receive command, set registers. Current consumption at Active is minimum.
2) Standby : State of waiting next AD conversion at Normal Mode. Able to receive command, set registers.
3) Warm : COM terminal switch specified for AD conversion is on.
4) Idle : Able to receive command, set registers, and access to NVM.
5) BootLoad /Reset : State to copy data from NVM to register after power-ON or reset, or state of ODET
6) Active (Normal) : State to convert AD at Normal Mode. Common name is "Normal Mode".
7) Active (Sequential) : State to convert AD at Sequential Mode. Common name is "Sequential Mode".

State transition

Table 14.1 State transition list

IC operation setting	State					
	Sleep	Standby	Warm	Idle	Active (Normal)	Active (Sequential)
Reset	○ Shift to each state depending on NVM setting after reset all register and BootLoad					
Sleep	○ (Keep)	○ Shift to Sleep	○ Shift to Sleep	○ Shift to Sleep	○ Shift to Sleep after AD conversion	○ Shift to Sleep after AD conversion
Standby	○ Shift to Standby	○ (Keep)	○ Shift to Standby	○ Shift to Standby	○ Shift to Standby after AD conversion	○ Shift to Standby after AD conversion
Warm	○ Shift to Warm	○ Shift to Warm	○ (Keep)	○ Shift to Warm	○ Shift to Warm after AD conversion	○ Shift to Warm after AD conversion
Idle	○ Shift to Idle	○ Shift to Idle	○ Shift to Idle	○ (Keep)	○ Shift to Idle after AD conversion	○ Shift to Idle after AD conversion
BootLoad	○ Shift to each state depending on NVM setting after BootLoad				○ (Prohibited when NVM Addr.81h bit[2:0] = 001b or 010b or 011b)	
Active (Normal)	○ Shift to Normal Mode	○ Shift to Normal Mode	○ Shift to Normal Mode	○ Shift to Normal Mode	○ (Keep)	○ Shift to Normal Mode after AD conversion
Active (Sequential)	○ Shift to Sequential Mode	○ Shift to Sequential Mode	○ Shift to Sequential Mode	○ Shift to Sequential Mode	○ Shift to Sequential Mode after AD conversion	○ (Keep)

*The operating mode setting except Reset command is not accepted during BootLoad.
**Reset by RSTB terminal is same as Reset command above table.

After power input, the digital circuit is reset using POR circuit with a built-in MV3830. After reset, BootLoad is executed. At this time, any register cannot be written through the communication line because NVM contents are read in the register. (Data can be read.) After BootLoad, MV3830 transfers to another status defined in Table 13.1 according to the value set in MODE [2:0] of register address 0Fh. Also, it transfers to appropriate state following the command sent from the host.
When an error occurs during the BootLoad, MV3830 waits in the Sleep state. One or both of ERR_CRC and ERR_INFO whose resister address is 09h are set to "1". For details of them, see Register map.

Hard-ware reset

RSTB terminal can reset hardware (entire digital circuit). After the reset of the hardware, MV3830 transfers to BootLoad.

REGISTER

Register address map

■Boot Load

For Address = 0Ch to 63h, data is read from NVM at Bootload.

■Access restriction

1) LV1: R / W is possible in the initial state. Registers accessible to end users
2) LV2: Depending on product deployment, there is a possibility of publication
3) LV3: Register that assumed to be used only for evaluation and inspection

Access method to LV 2, LV 3: See the section of register address 66h

Table 15.1 Register address map (1/3)

Item	Address	Init. Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Read	Write
RES_STACK1	00h	00h	RES_STACK1[23:16]								R	LV1	-
RES_STACK1	01h	00h	RES_STACK1[15:8]								R	LV1	-
RES_STACK1	02h	00h	RES_STACK1[7:0]								R	LV1	-
RES_STACK2	03h	00h	RES_STACK2[23:16]								R	LV1	-
RES_STACK2	04h	00h	RES_STACK2[15:8]								R	LV1	-
RES_STACK2	05h	00h	RES_STACK2[7:0]								R	LV1	-
RES_STACK3	06h	00h	RES_STACK3[23:16]								R	LV1	-
RES_STACK3	07h	00h	RES_STACK3[15:8]								R	LV1	-
RES_STACK3	08h	00h	RES_STACK3[7:0]								R	LV1	-
ST	09h	00h	*Reserve*	ERR_CRC	ERR_INFO	NVMLOAD	RDY_DATA	STATUS[2:0]			R	LV1	-
ST_SENSOR	0Ah	00h	*Reserve*	*Reserve*	*Reserve*	DONE_ODET	ERR_CH2	ERR_CH1	ERR_CH0_EXT	ERR_CH0_INT	R	LV1	-
ST_INFO	0Bh	08h or 48h	0	0 or 1	0	0	1	0	0	0	R	LV1	-
I2CADDR	***0Ch***	4Dh	*Reserve*	I2C ADDR[6:0]							R	LV1	-
FILT_SET	***0Dh***	00h	*Reserve*	*Reserve*	*Reserve*	SET_CRC	SELF_CHK	CIC_OSRALL	IIR_COEF[1:0]		RW	LV1	LV1
MEAS_EN	***0Eh***	00h	SET_SEQ[1:0]		EN_3RD[1:0]		EN_2ND[1:0]		EN_1ST[1:0]		RW	LV1	LV1
MEAS_CTRL	***0Fh***	00h	*Reserve*	TSTBY[2:0]			*Reserve*	MODE[2:0]			RW	LV1	LV1
GPOTH_1	***10h***	00h	SET_GPOTH[1:0]	GPOTH_DATA[13:8]							RW	LV1	LV1
GPOTH_0	***11h***	00h	GPOTH_DATA[7:0]								RW	LV1	LV1
CC_CH0_Z_1	***12h***	xxh	CC_CH0_Z[15:8]								RW	LV1	LV3
CC_CH0_Z_0	***13h***	xxh	CC_CH0_Z[7:0]								RW	LV1	LV3
CC_CH0_F_1	***14h***	xxh	CC_CH0_F[15:8]								RW	LV1	LV3
CC_CH0_F_0	***15h***	xxh	CC_CH0_F[7:0]								RW	LV1	LV3
CC_CH0_S_1	***16h***	xxh	CC_CH0_S[15:8]								RW	LV1	LV3
CC_CH0_S_0	***17h***	xxh	CC_CH0_S[7:0]								RW	LV1	LV3
CC_CH0_T_1	***18h***	xxh	CC_CH0_T[15:8]								RW	LV1	LV3
CC_CH0_T_0	***19h***	xxh	CC_CH0_T[7:0]								RW	LV1	LV3
CC_CH1_ZZ_1	***1Ah***	xxh	CC_CH1_ZZ[15:8]								RW	LV1	LV3
CC_CH1_ZZ_0	***1Bh***	xxh	CC_CH1_ZZ[7:0]								RW	LV1	LV3
CC_CH1_ZF_1	***1Ch***	xxh	CC_CH1_ZF[15:8]								RW	LV1	LV3
CC_CH1_ZF_0	***1Dh***	xxh	CC_CH1_ZF[7:0]								RW	LV1	LV3
CC_CH1_ZS_1	***1Eh***	xxh	CC_CH1_ZS[15:8]								RW	LV1	LV3
CC_CH1_ZS_0	***1Fh***	xxh	CC_CH1_ZS[7:0]								RW	LV1	LV3

Table 15.2 Register address map (2/3)

Item	Address	Init. Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Read	Write
CC_CH1_FZ_1	20h	xxh	CC_CH1_FZ[15:8]								RW	LV1	LV3
CC_CH1_FZ_0	21h	xxh	CC_CH1_FZ[7:0]								RW	LV1	LV3
CC_CH1_FF_1	22h	xxh	CC_CH1_FF[15:8]								RW	LV1	LV3
CC_CH1_FF_0	23h	xxh	CC_CH1_FF[7:0]								RW	LV1	LV3
CC_CH1_FS_1	24h	xxh	CC_CH1_FS[15:8]								RW	LV1	LV3
CC_CH1_FS_0	25h	xxh	CC_CH1_FS[7:0]								RW	LV1	LV3
CC_CH1_SZ_1	26h	xxh	CC_CH1_SZ[15:8]								RW	LV1	LV3
CC_CH1_SZ_0	27h	xxh	CC_CH1_SZ[7:0]								RW	LV1	LV3
CC_CH1_SF_1	28h	xxh	CC_CH1_SF[15:8]								RW	LV1	LV3
CC_CH1_SF_0	29h	xxh	CC_CH1_SF[7:0]								RW	LV1	LV3
CC_CH1_SS_1	2Ah	xxh	CC_CH1_SS[15:8]								RW	LV1	LV3
CC_CH1_SS_0	2Bh	xxh	CC_CH1_SS[7:0]								RW	LV1	LV3
CC_CH1_TZ_1	2Ch	xxh	CC_CH1_TZ[15:8]								RW	LV1	LV3
CC_CH1_TZ_0	2Dh	xxh	CC_CH1_TZ[7:0]								RW	LV1	LV3
CC_CH1_TF_1	2Eh	xxh	CC_CH1_TF[15:8]								RW	LV1	LV3
CC_CH1_TF_0	2Fh	xxh	CC_CH1_TF[7:0]								RW	LV1	LV3
CC_CH1_TS_1	30h	xxh	CC_CH1_TS[15:8]								RW	LV1	LV3
CC_CH1_TS_0	31h	xxh	CC_CH1_TS[7:0]								RW	LV1	LV3
CC_CH2_ZZ_1	32h	xxh	CC_CH2_ZZ[15:8]								RW	LV1	LV3
CC_CH2_ZZ_0	33h	xxh	CC_CH2_ZZ[7:0]								RW	LV1	LV3
CC_CH2_ZF_1	34h	xxh	CC_CH2_ZF[15:8]								RW	LV1	LV3
CC_CH2_ZF_0	35h	xxh	CC_CH2_ZF[7:0]								RW	LV1	LV3
CC_CH2_ZS_1	36h	xxh	CC_CH2_ZS[15:8]								RW	LV1	LV3
CC_CH2_ZS_0	37h	xxh	CC_CH2_ZS[7:0]								RW	LV1	LV3
CC_CH2_FZ_1	38h	xxh	CC_CH2_FZ[15:8]								RW	LV1	LV3
CC_CH2_FZ_0	39h	xxh	CC_CH2_FZ[7:0]								RW	LV1	LV3
CC_CH2_FF_1	3Ah	xxh	CC_CH2_FF[15:8]								RW	LV1	LV3
CC_CH2_FF_0	3Bh	xxh	CC_CH2_FF[7:0]								RW	LV1	LV3
CC_CH2_FS_1	3Ch	xxh	CC_CH2_FS[15:8]								RW	LV1	LV3
CC_CH2_FS_0	3Dh	xxh	CC_CH2_FS[7:0]								RW	LV1	LV3
CC_CH2_SZ_1	3Eh	xxh	CC_CH2_SZ[15:8]								RW	LV1	LV3
CC_CH2_SZ_0	3Fh	xxh	CC_CH2_SZ[7:0]								RW	LV1	LV3
CC_CH2_SF_1	40h	xxh	CC_CH2_SF[15:8]								RW	LV1	LV3
CC_CH2_SF_0	41h	xxh	CC_CH2_SF[7:0]								RW	LV1	LV3
CC_CH2_SS_1	42h	xxh	CC_CH2_SS[15:8]								RW	LV1	LV3
CC_CH2_SS_0	43h	xxh	CC_CH2_SS[7:0]								RW	LV1	LV3
CC_CH2_TZ_1	44h	xxh	CC_CH2_TZ[15:8]								RW	LV1	LV3
CC_CH2_TZ_0	45h	xxh	CC_CH2_TZ[7:0]								RW	LV1	LV3
CC_CH2_TF_1	46h	xxh	CC_CH2_TF[15:8]								RW	LV1	LV3
CC_CH2_TF_0	47h	xxh	CC_CH2_TF[7:0]								RW	LV1	LV3
CC_CH2_TS_1	48h	xxh	CC_CH2_TS[15:8]								RW	LV1	LV3
CC_CH2_TS_0	49h	xxh	CC_CH2_TS[7:0]								RW	LV1	LV3
CC_SET_SHIFT_C	4Ah	xxh	BITSHIFT_CH0_F[3:0]				BITSHIFT_CH0_S[3:0]				RW	LV1	LV3
CC_SET_SHIFT_B	4Bh	xxh	BITSHIFT_CH0_T[3:0]				BITSHIFT_CH1_ZF[3:0]				RW	LV1	LV3
CC_SET_SHIFT_A	4Ch	xxh	BITSHIFT_CH1_ZS[3:0]				BITSHIFT_CH1_FF[3:0]				RW	LV1	LV3
CC_SET_SHIFT_9	4Dh	xxh	BITSHIFT_CH1_FS[3:0]				BITSHIFT_CH1_F[3:0]				RW	LV1	LV3
CC_SET_SHIFT_8	4Eh	xxh	BITSHIFT_CH1_SF[3:0]				BITSHIFT_CH1_SS[3:0]				RW	LV1	LV3
CC_SET_SHIFT_7	4Fh	xxh	BITSHIFT_CH1_S[3:0]				BITSHIFT_CH1_TF[3:0]				RW	LV1	LV3
CC_SET_SHIFT_6	50h	xxh	BITSHIFT_CH1_TS[3:0]				BITSHIFT_CH1_T[3:0]				RW	LV1	LV3
CC_SET_SHIFT_5	51h	0xh	*Reserve*	*Reserve*	*Reserve*	*Reserve*	BITSHIFT_CH2_ZF[3:0]				RW	LV1	LV3
CC_SET_SHIFT_4	52h	xxh	BITSHIFT_CH2_ZS[3:0]				BITSHIFT_CH2_FF[3:0]				RW	LV1	LV3
CC_SET_SHIFT_3	53h	xxh	BITSHIFT_CH2_FS[3:0]				BITSHIFT_CH2_F[3:0]				RW	LV1	LV3
CC_SET_SHIFT_2	54h	xxh	BITSHIFT_CH2_SF[3:0]				BITSHIFT_CH2_SS[3:0]				RW	LV1	LV3
CC_SET_SHIFT_1	55h	xxh	BITSHIFT_CH2_S[3:0]				BITSHIFT_CH2_TF[3:0]				RW	LV1	LV3
CC_SET_SHIFT_0	56h	xxh	BITSHIFT_CH2_TS[3:0]				BITSHIFT_CH2_T[3:0]				RW	LV1	LV3

Table 15.3 Register address map (3/3)

Item	Address	Init. Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Read	Write
IO_SET	***57h***	00h	*Reserve*	*Reserve*	*Reserve*	*Reserve*	*Reserve*	SEL_RAW	SET_STAT	DIS_RES_WIDTH	RW	LV1	LV3
TRIM_VOFF1	***58h***	xxh	TRIM_VOFF1[7:0]								RW	LV1	LV3
TRIM_VOFF2	***59h***	xxh	TRIM_VOFF2[7:0]								RW	LV1	LV3
CH0_FILT	***5Ah***	00h	CH0_OSR[1:0]		CH0_AVG[2:0]			CH0_GAIN[2:0]			RW	LV1	LV3
CH1_FILT	***5Bh***	00h	CH1_OSR[1:0]		CH1_AVG[2:0]			CH1_GAIN[2:0]			RW	LV1	LV3
CH2_FILT	***5Ch***	00h	CH2_OSR[1:0]		CH2_AVG[2:0]			CH2_GAIN[2:0]			RW	LV1	LV3
CH_MISC_SET	***5Dh***	10h	*Reserve*	DIS_DEM_PGA	SET_DIFF	CON_VREFN	CH2_TYPE	CH1_TYPE	CH0_DISCON	CH0_SEL_EXTEMP	RW	LV1	LV3
TRIM1	***5Eh***	xxh	TRIM_LPVREF[3:0]				TRIM_LPOSC[3:0]				RW	LV1	LV3
TRIM2	***5Fh***	xxh	*Reserve*	*Reserve*	TRIM_BGR[5:0]						RW	LV1	LV3
TRIM3	***60h***	xxh	TRIM_IREF[3:0]				TRIM_RG[3:0]				RW	LV1	LV3
TRIM4	***61h***	xxh	SPD_OSC[1:0]		TRIM_OSC[5:0]						RW	LV1	LV3
MON_SET	***62h***	00h	DIS_FILT	*Reserve*	SEL_GPO[5:0]						RW	LV1	LV3
MISC_SET	***63h***	00h	SET_WARM	SET_ODET	SEL_CYC	EN_BI	TEST_ACT	SET_RGO[2:0]			RW	LV1	LV3
NVM_TEST1	64h	00h	BULK_ODD_EN	BULK_EVEN_EN	MREAD_EN	CCMON_EN	OSCMON_EN	MARGIN_TRIM[2:0]			RW	LV2	LV2
NVM_TEST2	65h	00h	VTUNMON_EN	CORE_IBIAS_OVR_EN	OSC_OVR_EN	OSC_IBIAS_MON_EN	*Reserve*	DIS_CP	DIS_PROG	DIS_ERASE	RW	LV2	LV2
ACCS_CTRL	66h	00h	*Reserve*	*Reserve*	*Reserve*	*Reserve*	*Reserve*	EN_LV3	CTL_EN_LV3	EN_LV2	RW	LV2	Special

Details of register address map

RES_STACK1/2/3 (Addr. = 00h to 08h)

Table 15.4 Register address map (1/25)

Address	Initial Val.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
[Result Register]										
00h to 02h (RES_STACK1)	00h	RES_STACK1[23:0] Corrected sensor conversion result stored in STACK1								R/- LV1/-
03h to 05h (RES_STACK2)	00h	RES_STACK2[23:0] Corrected sensor conversion result stored in STACK2								R/- LV1/-
06h to 08h (RES_STACK3)	00h	RES_STACK3[23:0] Corrected sensor conversion result stored in STACK3								R/- LV1/-

Order of sensor: The order of sensor measurement is specified in register MEAS_EN (Addr.=0Eh).
Measurement The sensors set in this register are measured in the order of EN_1ST, EN_2ND, and EN_3RD.

Data storage: Because of the use of stack structure, stored data is as shown below:

Result Register	Stored data		
	Number of sensors to be measured =1	Number of sensors to be measured =2	Number of sensors to be measured =3
RES_STACK1[23:0]	Result of sensor set with EN_1ST	Result of sensor set with EN_2ND	Result of sensor set with EN_3RD
RES_STACK2[23:0]	00h (Initial value)	Result of sensor set with EN_1ST	Result of sensor set with EN_2ND
RES_STACK3[23:0]	00h (Initial value)	00h (Initial value)	Result of sensor set with EN_1ST

The stored data measured in the Sequential Mode is as shown below. To retrieve temperature-compensated physical value, it is necessary to retrieve temperature value in Normal Mode before measuring physical value in Sequential Mode.

Result Register	Stored data	
	First, the temperature is measured in the Normal Mode.	Next, physical quantities are measured in the Sequential Mode.
RES_STACK1[23:0]	Temperature conversion result	Physical value conversion result
RES_STACK2[23:0]	(Default)	Temperature conversion result
RES_STACK3[23:0]	(Default)	(Default)

For output data format, see Retrieve temperature and physical value.

ST (Addr. = 09h)

Table 15.5 Register address map (2/25)

Address	Initial Val.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
[Control Register]										
09h (ST)	00h	Reserve	ERR_CRC	ERR_INFO	NVMLOAD	RDY_DATA	STATUS[2:0]			R/-
		ERR_CRC: NVM CRC error detection signal. 0: Normal, 1: Abnormal When this is "1" (Abnormal), this IC becomes Sleep, the I2C address is set to initial value 4Dh, and the IC cannot shift to except Reset. And sensor connection detection isn't active, too. Clear condition: Reset or setting of "0" while the access restriction is LV3 ERR_INFO: Signal informing prohibition setting (below). 0: Normal, 1: Abnormal 1) NVM MODE [2:0] is set to 100b (Reset), or 110b (BootLoad). 2) Prohibition setting in CHx_SET is made. 3) No state transition was available. Clear condition: Reset or cleared when this register is no longer prohibited. NVMLOAD: During BootLoad, data transfer detection signal from NVM to REG. 0: data transfer, 1: other status. Clear condition: End of data transfer or Reset RDY_DATA: Signal determining acquisition of conversion result This bit is "0" in the state before AD conversion execution after power-on or reset, and "1" after AD conversion completion. Also, when AD conversion result is acquired from the result resister while this bit is "1", it is set to"0". STATUS [2:0]: Represents IC status. 000b: Sleep 001b: Active (Normal) 010b: Active (Sequential) 011b: Idle 100b: None (Including during state transition) 101b: Standby 110b: BootLoad 111b: Warm								LV1 /-

ST_SENSOR (Addr. = 0Ah)

Table 15.6 Register address map (3/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0Ah (ST_SENSOR)	00h	Reserve			DONE_ODET	ERR_CH2	ERR_CH1	ERR_CH0_EXT	ERR_CH0_INT	R/-
	DIGI _AON	DONE_ODET: Signal to notify completion of detection phase in sensor connection detection circuit. After power input, "0" is set. After completion of the detection phase, "1" is set. This is fixed to "0" when SET_ODET is 0b. This bit can be cleared by resetting IC itself (H/W Reset, S/W Reset) or by setting "0" when access restriction is LV3. ERR_CH* shown below is a signal to notify that the sensor open status is detected, and the open status is detected as abnormal. Therefore, when sensor connection detection is activated while no sensor is connected such as during IC evaluation, an abnormal status is detected. This bit can be cleared by resetting IC itself (H/W Reset, S/W Reset) or by setting "0" when access restriction is LV3. ERR_CH2: Channel 2 (A2P, A2M, COM2) sensor connection detection result (1: Abnormal, 0: Normal) ERR_CH1: Channel 1 (A1P, A1M, COM1) sensor connection detection result (1: Abnormal, 0: Normal) ERR_CH0_EXT: External channel 0 (A0P, A0M, COM0) sensor connection detection result (1: Abnormal, 0: Normal) ERR_CH0_INT: Internal channel 0 sensor connection detection result (1: Abnormal, 0: Normal)									LV1/ -

ST_INFO (Addr. = 0Bh)

Table 15.7 Register address map (4/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0Bh (ST_INFO)	08h or 48h	0	0 or 1	0	0	1	0	0	0	R/-
	DIGI _AON	Setting information of IC operation mode. IC's normal operation can be confirmed by checking this information before AD conversion. Values read in Sleep mode are as follows: Internal regulator activation mode: bit[7:0] = 0000_1000b External VRG applying mode: bit[7:0] = 0100_1000b								LV1/ -

I2CADDR (Addr. = 0Ch)

Table 15.8 Register address map (5/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0Ch (I2CADDR)	4Dh	Reserve	I2CADDRES[6:0]							R/-
	DIGI _AON	I2CADDR [6:0]: I2C address can be confirmed.								LV1/ -

FILT_SET (Addr. = 0Dh)

Table 15.9 Register address map (6/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0Dh (FILT_ SET)	00h	Reserve			SET_CRC	SELF_CHK	CIC_OSRALL	IIR_COEF[1:0]		R/W
	DIGI _AON	SET_CRC: CRC addition function to detect accidental data error of I2C communication. "0" is a standard setting and no CRC function. "1" is enable CRC function and add CRC for I2C communication. SELF_CHK: Controls self-diagnosis mode. "0" is a standard setting and specifies the normal operation. When "1" is set and "Normal Mode command is executed, the self-diagnosis mode starts. In this mode, the internally generated voltage (fixed value) is AD converted. The conversion result enables to determine the presence or absence of a failure in ADC peripheral circuit. $Check\ result = RES\_STACK1 \div RES\_STACK2$ $1.9 < Check\ result < 2.1 \Rightarrow Normal$ $Check\ result < 1.9,\ 2.1 < Check\ result \Rightarrow Abnormal$ Fig. 15.1 Controls self-diagnosis mode shows the operation flowchart. CIC_OSRALL: Uniformly sets OSR value of each CH. 0: Standard setting (Setting of CH0_OSR/CH1_OSR/CH2_OSR of Addr.=5Ah/5Bh/5Ch is valid.) 1: Average current is reduced by making OSR value one level lower than standard setting. Note: This bit is invalid when OSR value is 00b because this is the minimum setting. CIC_OSRALL should be set during Sleep, Standby, and Warm. Specifies IIR filter coefficient (coef_filter). This setting changes output responsiveness and input conversion noise. This filter is intended to be used in the Sequential Mode. 00b: filter Off 01b: coef_filter = 2 10b: coef_filter = 4 11b: coef_filter = 8 $data\_filter = \frac{data\_filter\_old \cdot (coef\_filter - 1) + data\_ADC}{coef\_filter}$ The following restrictions should be observed when using IIR filters. (1) When using Normal Mode, be sure to disable the IIR filter. (2) IIR_COEF should be set during Sleep, Standby, and Warm. (3) Be sure to transition to Sleep, Standby, or Warm at the end of Sequential Mode using the IIR filter.								LV1/ LV1

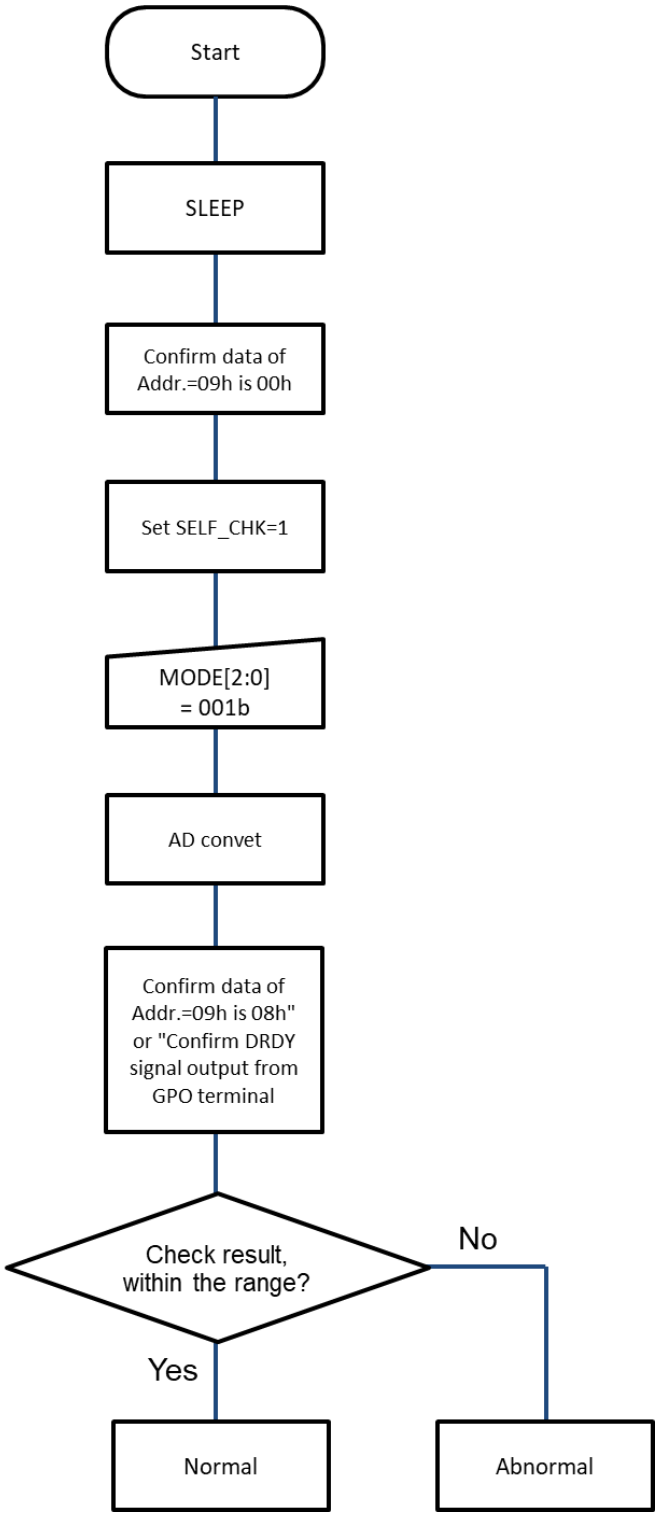


Fig. 15.1 Controls self-diagnosis mode operation flowchart

MEAS_EN (Addr. = 0Eh)

Table 15.10 Register address map (7/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0Eh (MEAS_EN)	00h	SET_SEQ[1:0]		EN_3RD[1:0]		EN_2ND[1:0]		EN_1ST[1:0]		R/W
	DIGI _AON	SET_SEQ [1:0]: Specifies a measurement target in the Sequential Mode. 00b: No target (ERR_INFO set to "1" when not execute AD conversion by setting MODE [2:0] to 010b while this setting is made.) 01b: Temperature sensor connected to CH0 Temperature sensors are specified in CH0_SEL_EXTEMP of CH_MISC_SET (Addr. =5Dh). 10b: Sensor connected to CH1 Sensor types are specified in CH1_TYPE of CH_MISC_SET (Addr. =5Dh). 11b: Sensor connected to CH2 Sensor types are specified in CH2_TYPE of CH_MISC_SET (Addr. =5Dh). EN_1ST [1:0]: Specifies the first measurement target in the Normal Mode. 00b: No target 01b: Temperature sensor connected to CH0 Temperature sensors are specified in CH0_SEL_EXTEMP of CH_MISC_SET (Addr. =5Dh). 10b: Sensor connected to CH1 Sensor types are specified in CH1_TYPE of CH_MISC_SET (Addr. =5Dh). 11b: Sensor connected to CH2 Sensor types are specified in CH2_TYPE of CH_MISC_SET (Addr. =5Dh). EN_2ND [1:0]: Specifies the second measurement target in the Normal Mode. For detail settings, refer to the description of register EN_1ST [1:0]. EN_3RD [1:0]: Specifies the third measurement target in the Normal Mode. For detail settings, refer to the description of register EN_1ST [1:0]. ERR_INFO set to "1" when not execute AD conversion by setting MODE [2:0] to 001b while EN_1ST [1:0] =00b and EN_2ND [1:0] =00b and EN_3RD [1:0] =00b.							LV1/ LV1

MEAS_CTRL (Addr. = 0Fh)

Table 15.11 Register address map (8/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0Fh (MEAS_CTRL)	00h	Reserve	TSTBY[2:0]			Reserve	***MODE[2:0]***			R/W
	DIGI _AON	TSTBY [2:0]: Specifies standby time in the Normal Mode. 000b: 0ms 001b: 10ms 010b: 100ms 011b: 400ms 100b: 1000ms 101b: 1000ms 110b: 1000ms 111b: One Shot Transition state after AD conversion command in which the standby time is set to "One Shot" changes by the setting SET_WARM (Addr. = 63h). Transition state after AD conversion is shown below. ■SET_WARM=0 Shift to Sleep ■SET_WARM=1 Transition state after AD conversion changes depending on the state of executing AD conversion command. ① Shift to Sleep: Sleep, Idle ② Shift to Warm: Active(Normal), Active(Sequential), Standby, Warm And, when the standby time is set to "One Shot", and the IC operating setting is set to "Normal Mode", the IC shift to Warm after AD conversion MODE [2:0]: Specifies the IC operation. The time between execution Reset or BootLoad commands and the next command execution should be 4ms or more when SEL_CYC=0, 28.5ms or more when SEL_CYC=1.If you don't use DRDY, the time from issuing the Sequential Mode command to acquiring data should be 2 msec or more. 000b: Sleep 001b: Active(Normal) Measurement target must be specified in MEAS_EN bit [5:0] beforehand. 010b :Active(Sequential) Measurement target must be specified in MEAS_EN bit [7:6] beforehand. 011b: Idle 100b: Reset 101b: Standby 110b: BootLoad If NVM Addr. = 81h bit [2:0] is 001b, 010b, or 011b, do not issue during Active. 111b: Warm								LV1/ LV1

GPOTH (Addr. = 10h～11h)

Table 15.12 Register address map (9/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
10h (GPOTH_1)	00h	SET_GPOTH[1:0]		GPOTH_DATA[13:8]						R/W
	DIGI _AON	SET_GPOTH [1:0]: Controls output signals from GPO terminal. When this terminal outputs the AD conversion complete flag DRDY (B), this IC can output signals to the host. This IC allows the GPO to output a signal only when a correction value (RES_STACK) is beyond the specified threshold (GPOTH_DATA). These bits specifies the correction value to calculate. Details of this function are given outside the box. : 00b: No comparison with RES_STACK value (Signals are always output from GPO.) 01b: Comparison with RES_STACK1 value 10b: Comparison with RES_STACK2 value 11b: Comparison with RES_STACK3 value GPOTH_DATA [13:8]: Specifies the threshold of RES_STACK value by making data 14-bits width in combination with GPOTH_DATA [7:0].								LV1/ LV1
11h (GPOTH_0)	00h	GPOTH_DATA[7:0]								R/W
	DIGI _AON	Specifies the threshold in combination with GPOTH_DATA [13:8].								LV1/ LV1

This register realizes the following functions.

■Outline

Correction value (RES_STACK value) > Threshold (GPOTH_DATA value) Pulse output from GPO
Correction value (RES_STACK value) ≤ Threshold (GPOTH_DATA value) No pulse output from GPO

■GPO setting

・ Resistor MON_SET SEL_GPO[5:0] = 6’b01_1000
・ Resistor MON_SET SEL_GPO[5:0] = 6’b01_1001

■GPO output judgment

Correction value (RES_STACK value) > Threshold (GPOTH_DATA value)・・・Pulse output from GPO
Correction value (RES_STACK value) ≤ Threshold (GPOTH_DATA value)・・・No pulse output from GPO

Note: that the above RES_STACK value is RES_STACK*[23:10].

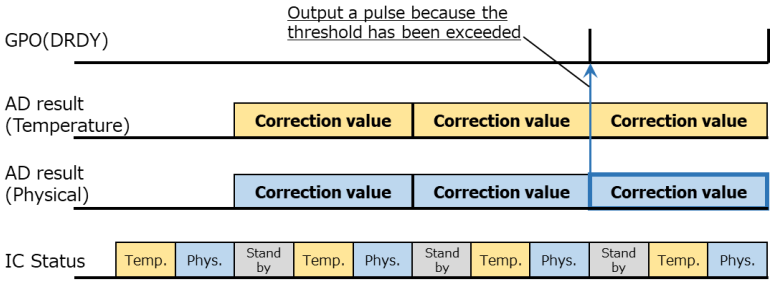


Fig. 15.2 Output of signal

CC (Addr. = 12h～49h)

Table 15.13 Register address map (10/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
12h-13h (CC_CH0_Z)	xxh	CC_CH0_Z[15:0]								R/W
	DIGI_AON	CC_CH0_Z[15:0] : Zero order correction coefficient for temperature sensor connected to CH0.								LV1/ LV3
14h-15h (CC_CH0_F)	xxh	CC_CH0_F[15:0]								R/W
	DIGI_AON	CC_CH0_F[15:0] : 1st order correction coefficient for temperature sensor connected to CH0.								LV1/ LV3
16h-17h (CC_CH0_S)	xxh	CC_CH0_S[15:0]								R/W
	DIGI_AON	C_CH0_S[15:0] : 2nd order correction coefficient for temperature sensor connected to CH0.								LV1/ LV3
18h-19h (CC_CH0_T)	xxh	CC_CH0_T[15:0]								R/W
	DIGI_AON	CC_CH0_T[15:0] : 3rd order correction coefficient for temperature sensor connected to CH0.								LV1/ LV3
1Ah-1Bh (CC_CH1_ZZ)	xxh	CC_CH1_ZZ[15:0]								R/W
	DIGI_AON	CC_CH1_ZZ[15:0] : Offset temperature characteristic zero order coefficient for the sensor connected to CH1 or zero order correction coefficient for temperature sensor connected to CH1.								LV1/ LV3
1Ch-1Dh (CC_CH1_ZF)	xxh	CC_CH1_ZF[15:0]								R/W
	DIGI_AON	CC_CH1_ZF[15:0] : Offset temperature characteristic 1st order coefficient for the sensor connected to CH1 or 1st order correction coefficient for temperature sensor connected to CH1.								LV1/ LV3
1Eh-1Fh (CC_CH1_ZS)	xxh	CC_CH1_ZS[15:0]								R/W
	DIGI_AON	CC_CH1_ZS[15:0] : Offset temperature characteristic 2nd order coefficient for the sensor connected to CH1 or 2nd order correction coefficient for temperature sensor connected to CH1.								LV1/ LV3
20h-21h (CC_CH1_FZ)	xxh	CC_CH1_FZ[15:0]								R/W
	DIGI_AON	CC_CH1_FZ[15:0] : 1st order temperature characteristic zero order coefficient for the sensor connected to CH1 or 3rd order correction coefficient for temperature sensor connected to CH1.								LV1/ LV3
22h-23h (CC_CH1_FF)	xxh	CC_CH1_FF[15:0]								R/W
	DIGI_AON	CC_CH1_FF[15:0] : 1st order temperature characteristic 1st order coefficient for the sensor connected to CH1.								LV1/ LV3
24h-25h (CC_CH1_FS)	xxh	CC_CH1_FS[15:0]								R/W
	DIGI_AON	CC_CH1_FS[15:0] : 1st order temperature characteristic 2nd order coefficient for the sensor connected to CH1.								LV1/ LV3
26h-27h (CC_CH1_SZ)	xxh	CC_CH1_SZ[15:0]								R/W
	DIGI_AON	CC_CH1_SZ[15:0] : 2nd order temperature characteristic zero order coefficient for the sensor connected to CH1.								LV1/ LV3
28h-29h (CC_CH1_SF)	xxh	CC_CH1_SF[15:0]								R/W
	DIGI_AON	CC_CH1_SF[15:0] : 2nd order temperature characteristic 1st order coefficient for the sensor connected to CH1.								LV1/ LV3
2Ah-2Bh (CC_CH1_SS)	xxh	CC_CH1_SS[15:0]								R/W
	DIGI_AON	CC_CH1_SS[15:0] : 2nd order temperature characteristic 2nd order coefficient for the sensor connected to CH1.								LV1/ LV3

Table 15.14 Register address map (11/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
2Ch-2Dh (CC_CH1_TZ)	xxh	CC_CH1_TZ[15:0]								R/W
	DIGI_AON	CC_CH1_TZ[15:0] : 3rd order temperature characteristic zero order coefficient for the sensor connected to CH1.								LV1/ LV3
2Eh-2Fh (CC_CH1_TF)	xxh	CC_CH1_TF[15:0]								R/W
	DIGI_AON	CC_CH1_TF[15:0] : 3rd order temperature characteristic 1st order coefficient for the sensor connected to CH1.								LV1/ LV3
30h-31h (CC_CH1_TS)	xxh	CC_CH1_TS[15:0]								R/W
	DIGI_AON	CC_CH1_TS[15:0] : 3rd order temperature characteristic 2nd order coefficient for the sensor connected to CH1.								LV1/ LV3
32h-33h (CC_CH2_ZZ)	xxh	CC_CH2_ZZ[15:0]								R/W
	DIGI_AON	CC_CH2_ZZ[15:0] : Offset temperature characteristic zero order coefficient for the sensor connected to CH2.								LV1/ LV3
34h-35h (CC_CH2_ZF)	xxh	CC_CH2_ZF[15:0]								R/W
	DIGI_AON	CC_CH2_ZF[15:0] : Offset temperature characteristic 1st order coefficient for the sensor connected to CH2.								LV1/ LV3
36h-37h (CC_CH2_ZS)	xxh	CC_CH2_ZS[15:0]								R/W
	DIGI_AON	CC_CH2_ZS[15:0] : Offset temperature characteristic 2nd order coefficient for the sensor connected to CH2.								LV1/ LV3
38h-39h (CC_CH2_FZ)	xxh	CC_CH2_FZ[15:0]								R/W
	DIGI_AON	CC_CH2_FZ[15:0] : 1st order temperature characteristic zero order coefficient for the sensor connected to CH2.								LV1/ LV3
3Ah-3Bh (CC_CH2_FF)	xxh	CC_CH2_FF[15:0]								R/W
	DIGI_AON	CC_CH2_FF[15:0] : 1st order temperature characteristic 1st order coefficient for the sensor connected to CH2.								LV1/ LV3
3Ch-3Dh (CC_CH2_FS)	xxh	CC_CH2_FS[15:0]								R/W
	DIGI_AON	CC_CH2_FS[15:0] : 1st order temperature characteristic 2nd order coefficient for the sensor connected to CH2.								LV1/ LV3
3Eh-3Fh (CC_CH2_SZ)	xxh	CC_CH2_SZ[15:0]								R/W
	DIGI_AON	CC_CH2_SZ[15:0] : 2nd order temperature characteristic zero order coefficient for the sensor connected to CH2.								LV1/ LV3
40h-41h (CC_CH2_SF)	xxh	CC_CH2_SF[15:0]								R/W
	DIGI_AON	CC_CH2_SF[15:0] : 2nd order temperature characteristic 1st order coefficient for the sensor connected to CH2.								LV1/ LV3
42h-43h (CC_CH2_SS)	xxh	CC_CH2_SS[15:0]								R/W
	DIGI_AON	CC_CH2_SS[15:0] : 2nd order temperature characteristic 2nd order coefficient for the sensor connected to CH2.								LV1/ LV3

Table 15.15 Register address map (12/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
44h-45h (CC_CH2_TZ)	xxh	CC_CH2_TZ[15:0]								R/W
	DIGI _AON	CC_CH2_TZ[15:0] : 3rd order temperature characteristic zero order coefficient for the sensor connected to CH2.								LV1/ LV3
46h-47h (CC_CH2_TF)	xxh	CC_CH2_TF[15:0]								R/W
	DIGI _AON	CC_CH2_TF[15:0] : 3rd order temperature characteristic 1st order coefficient for the sensor connected to CH2.								LV1/ LV3
48h-49h (CC_CH2_TS)	xxh	CC_CH2_TS[15:0]								R/W
	DIGI _AON	CC_CH2_TS[15:0] : 3rd order temperature characteristic 2nd order coefficient for the sensor connected to CH2.								LV1/ LV3

CC_SET_SHIFT (Addr. = 4Ah～56h)

Table 15.16 Register address map (13/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
4Ah (CC_SET_ SHIFT_C)	xxh	BITSHIFT_CH0_F[3:0]				BITSHIFT_CH0_S[3:0]				R/W
	DIGI _AON	BITSHIFT_CH0_F[3:0] : In correction calculation, specifies the shift amount when multiplying 1st order correction coefficient for temperature sensor connected to CH0 and the AD value. BITSHIFT_CH0_S[3:0] : In correction calculation, specifies the shift amount when multiplying 2nd order correction coefficient for temperature sensor connected to CH0 and the AD value.								LV1/ LV3
4Bh (CC_SET_ SHIFT_B)	xxh	BITSHIFT_CH0_T[3:0]				BITSHIFT_CH1_ZF[3:0]				R/W
	DIGI _AON	BITSHIFT_CH0_T[3:0] : In correction calculation, specifies the shift amount when multiplying 3rd order correction coefficient for temperature sensor connected to CH0 and the AD value. BITSHIFT_CH1_ZF[3:0] : In correction calculation, specifies the shift amount when multiplying offset temperature characteristic 1st order coefficient for the sensor connected to CH1 and the corrected temperature AD value or specifies the shift amount when multiplying 1st order correction coefficient for temperature sensor connected to CH1 and the AD value.								LV1/ LV3
4Ch (CC_SET_ SHIFT_A)	xxh	BITSHIFT_CH1_ZS[3:0]				BITSHIFT_CH1_FF[3:0]				R/W
	DIGI _AON	BITSHIFT_CH1_ZS[3:0] : In correction calculation, specifies the shift amount when multiplying offset temperature characteristic 2nd order coefficient for the sensor connected to CH1 and the corrected temperature AD value or specifies the shift amount when multiplying 2nd order correction coefficient for temperature sensor connected to CH1 and the AD value. BITSHIFT_CH1_FF[3:0] : In correction calculation, specifies the shift amount when multiplying 1st order temperature characteristic 1st order coefficient for the sensor connected to CH1 and the corrected temperature AD value or specifies the shift amount when multiplying 3rd order correction coefficient for temperature sensor connected to CH1 and the AD value.								LV1/ LV3

Table 15.17 Register address map (14/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
4Dh (CC_SET_ SHIFT_9)	xxh	BITSHIFT_CH1_FS[3:0]				BITSHIFT_CH1_F[3:0]				R/W
	DIGI _AON	BITSHIFT_CH1_FS[3:0] : In correction calculation, specifies the shift amount when multiplying 1st order temperature characteristic 2nd order coefficient for the sensor connected to CH1 and the corrected temperature AD value. BITSHIFT_CH1_F[3:0] : In correction calculation, specifies the shift amount when multiplying 1st order coefficient for the sensor connected to CH1 and the AD value.								LV1/ LV3
4Eh (CC_SET_ SHIFT_8)	xxh	BITSHIFT_CH1_SF[3:0]				BITSHIFT_CH1_SS[3:0]				R/W
	DIGI _AON	BITSHIFT_CH1_SF[3:0] : In correction calculation, specifies the shift amount when multiplying 2nd order temperature characteristic 1st order coefficient for the sensor connected to CH1 and the corrected temperature AD value. BITSHIFT_CH1_SS[3:0] : In correction calculation, specifies the shift amount when multiplying 2nd order temperature characteristic 2nd order coefficient for the sensor connected to CH1 and the corrected temperature AD value.								LV1/ LV3
4Fh (CC_SET_ SHIFT_7)	xxh	BITSHIFT_CH1_S[3:0]				BITSHIFT_CH1_TF[3:0]				R/W
	DIGI _AON	BITSHIFT_CH1_S[3:0] : In correction calculation, specifies the shift amount when multiplying 2nd order coefficient for the sensor connected to CH1 and the AD value. BITSHIFT_CH1_TF[3:0] : In correction calculation, specifies the shift amount when multiplying 3rd order temperature characteristic 1st order coefficient for the sensor connected to CH1 and the corrected temperature AD value.								LV1/ LV3
50h (CC_SET_ SHIFT_6)	xxh	BITSHIFT_CH1_TS[3:0]				BITSHIFT_CH1_T[3:0]				R/W
	DIGI _AON	BITSHIFT_CH1_TS[3:0] : In correction calculation, specifies the shift amount when multiplying 3rd order temperature characteristic 2nd order coefficient for the sensor connected to CH1 and the corrected temperature AD value. BITSHIFT_CH1_T[3:0] : In correction calculation, specifies the shift amount when multiplying 3rd order coefficient for the sensor connected to CH1 and the AD value.								LV1/ LV3
51h (CC_SET_ SHIFT_5)	xxh	Reserve				BITSHIFT_CH2_ZF[3:0]				R/W
	DIGI _AON	BITSHIFT_CH2_ZF[3:0] : In correction calculation, specifies the shift amount when multiplying offset temperature characteristic 1st order coefficient for the sensor connected to CH2 and the corrected temperature AD value.								LV1/ LV3

Table 15.18 Register address map (15/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
52h (CC_SET_ SHIFT_4)	xxh	BITSHIFT_CH2_ZS[3:0]				BITSHIFT_CH2_FF[3:0]				R/W
	DIGI _AON	BITSHIFT_CH2_ZS[3:0] : In correction calculation, specifies the shift amount when multiplying offset temperature characteristic 2nd order coefficient for the sensor connected to CH2 and the corrected temperature AD value or specifies the shift amount when multiplying 2nd order correction coefficient for temperature sensor connected to CH2 and the AD value. BITSHIFT_CH2_FF[3:0] : In correction calculation, specifies the shift amount when multiplying 1st order temperature characteristic 1st order coefficient for the sensor connected to CH2 and the corrected temperature AD value or specifies the shift amount when multiplying 3rd order correction coefficient for temperature sensor connected to CH2 and the AD value.								LV1/ LV3
53h (CC_SET_ SHIFT_3)	xxh	BITSHIFT_CH2_FS[3:0]				BITSHIFT_CH2_F[3:0]				R/W
	DIGI _AON	BITSHIFT_CH2_FS[3:0] : In correction calculation, specifies the shift amount when multiplying 1st order temperature characteristic 2nd order coefficient for the sensor connected to CH2 and the corrected temperature AD value. BITSHIFT_CH2_F[3:0] : In correction calculation, specifies the shift amount when multiplying 1st order coefficient for the sensor connected to CH2 and the AD value.								LV1/ LV3
54h (CC_SET_ SHIFT_2)	xxh	BITSHIFT_CH2_SF[3:0]				BITSHIFT_CH1_SS[3:0]				R/W
	DIGI _AON	BITSHIFT_CH2_SF[3:0] : In correction calculation, specifies the shift amount when multiplying 2nd order temperature characteristic 1st order coefficient for the sensor connected to CH2 and the corrected temperature AD value. BITSHIFT_CH2_SS[3:0] : In correction calculation, specifies the shift amount when multiplying 2nd order temperature characteristic 2nd order coefficient for the sensor connected to CH2 and the corrected temperature AD value.								LV1/ LV3
55h (CC_SET_ SHIFT_1)	xxh	BITSHIFT_CH2_S[3:0]				BITSHIFT_CH2_TF[3:0]				R/W
	DIGI _AON	BITSHIFT_CH2_S[3:0] : In correction calculation, specifies the shift amount when multiplying 2nd order coefficient for the sensor connected to CH2 and the AD value. BITSHIFT_CH2_TF[3:0] : In correction calculation, specifies the shift amount when multiplying 3rd order temperature characteristic 1st order coefficient for the sensor connected to CH2 and the corrected temperature AD value.								LV1/ LV3

Table 15.19 Register address map (16/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
56h (CC_SET_ SHIFT_0)	xxh	BITSHIFT_CH2_TS [3:0]				BITSHIFT_CH2_T[3:0]				R/W
	DIGI _AON	BITSHIFT_CH2_TS [3:0]: In correction calculation, specifies the shift amount when multiplying 3rd order temperature characteristic 2nd order coefficient for the sensor connected to CH2 and the corrected temperature AD value. BITSHIFT_CH2_T [3:0]: In correction calculation, specifies the shift amount when multiplying 3rd order coefficient for the sensor connected to CH2 and the AD value.								LV1/ LV3

IO_SET (Addr. = 57h)

Table 15.20 Register address map (17/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
57h (IO_SET)	00h	Reserve					SEL_RAW	SET_STAT	DIS_RES_WIDTH	R/W
	DIGI _AON	SEL_RAW: Specifies data to be stored in result registers (Addr. = 00h to 08h). 0: Post-correction data 1: Pre-correction data Don't change this bit during Active. When this bit is set to "1", bit1, 0 "SET_STAT, DIS_RES_WIDTH" is ignored. The bit is specified as 24bits and 2's complement. SET_STAT: Specifies whether to include status in the read data during execution of result read command. 0b: Status is not included in the start of read data. (24-/16-bits measurement result can be obtained.) 1b: Status is included in the start of read data. (Status and 22-/14-bits measurement result can be obtained. Two low-order bits are omitted.) If status is included, the following status is embedded in top two bits. 00b: New data 01b: Old data that has acquired once In addition, after power on or reset, the status when you execute result read command before AD conversion is "01b". DIS_RES_WIDTH: Specifies the bit width to read during execusion of result read command. 0b: The bit width is fixed as follows: Internal Temp Sensor: 16bits Resistance bridge sensor: 24bits Unspecified: 24bits 1b: The bit is specified as 24 bits.									LV1/ LV3

TRIM_VOFF (Addr. = 58h～59h)

Table 15.21 Register address map (18/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
58h (TRIM_VOFF1)	xxh	TRIM_VOFF1 [7:0]								R/W
	DIGI _AON	TRIM_VOFF1 [7:0]: Regulates offset voltage of Channel 1 connection sensor. The set value is 2's complement and the regulation range is Typ. -50mV/V to +50mV/V (0.4mV/V/step). When CH1_GAIN [2:0] =000b or 001b, this function is disable.								LV1/ LV3
59h (TRIM_VOFF2)	xxh	TRIM_VOFF2 [7:0]								R/W
	DIGI _AON	TRIM_VOFF2 [7:0]: Regulates offset voltage of Channel 2 connection sensor. The set value is 2's complement and the regulation range is Typ. -50mV/V to +50mV/V (0.4mV/V/step). When CH2_GAIN [2:0] =000b or 001b, this function is disable.								LV1/ LV3

CHx_FILT (Addr. = 5Ah～5Ch)

Table 15.22 Register address map (19/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
5Ah (CH0_FILT)	00h	CH0_OSR[1:0]		CH0_AVG[2:0]			CH0_GAIN[2:0]			R/W
	DIGI _AON	This address should be set during Sleep, Standby, and Warm. CH0_OSR [1:0]: Specifies CIC decimation ratio of CH0. 00b: 256 01b: 512 10b: 1024 11b: 2048 CH0_AVG [2:0]: Specifies the number of averaging times of CH0 measurement result. 000b: 1 001b: 2, right 1 bit shift 010b: 3, right 1 bit shift 011b: 4, right 2 bit shift 100b: 5, right 2 bit shift 101b: 6, right 2 bit shift 110b: 7, right 2 bit shift 111b: 8, right 3 bit shift CH0_GAIN [2:0]: Specifies pre-amplifier gain of CH0. 001b: 1 (go through the buffer in PGA for it TEST) 010b: 4 011b: 8 100b: 16 101b: 32 110b: 64 111b: 128								LV1/ LV3
5Bh (CH1_FILT)	00h	CH1_OSR[1:0]		CH1_AVG[2:0]			CH1_GAIN[2:0]			R/W
	DIGI _AON	Setting of CH1 filter and amplifier. For details, see register CH0_FILT.								LV1/ LV3
5Ch (CH2_FILT)	00h	CH2_OSR[1:0]		CH2_AVG[2:0]			CH2_GAIN[2:0]			R/W
	DIGI _AON	Setting of CH2 filter and amplifier. For details, see register CH0_FILT.								LV1/ LV3

CH_MISC_SET (Addr. = 5Dh)

Table 15.23 Register address map (20/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
5Dh (CH_MISC_ SET)	10h	Reserve	DIS_DE M_PGA	SET_DI FF	CON_VR EFN	CH2_TY PE	CH1_TY PE	CH0_DI SCON	CH0_SE L_EXTE MP	R/W
	DIGI _AON	DIS_DEM_PGA: For IC test SET_DIFF: This IC has a function to output a difference between two AD conversion results as one result (difference mode operation). This bit specifies the difference mode operation (0: Normal operation, 1: Difference mode operation). The calculation target is as follows, and only calculation result is stored in RES_STACK. Please specify SEL_RAW = 0 during difference mode operation. CON_VREFN: VREFN selection signal for ADC 0: Directly connects to VREFN terminal (For IC test) 1: Connects to COMx terminal CH2_TYPE: Specifies a sensor to be connected to CH2. 0b: Physical sensor (Resistance bridge type) 1b: Temperature sensor CH1_TYPE: Specifies a sensor to be connected to CH1. 0b: Physical sensor (Resistance bridge type) 1b: Temperature sensor CH0_DISCON: Specifies the signal to be additionally connected to the A0M terminal during CH0 conversion. This setting is used when the external temperature sensor connected to CH0 is single input, setting "0" connects unused ADC minus input to GND. 0b: Connects GND (Connect A0M terminal to GND inside IC). Specifically, Set to GND during CH0 conversion. 1b: No connection (A0M terminal is open inside IC. Bias voltage needs to be applied from the outside.) CH0_SEL_EXTEMP: Specifies a temperature sensor to be connected to CH0. 0b: Internal temperature sensor 1b: External temperature sensor								LV1/ LV3

In the difference mode controlled by SET_DIFF of Register CH_MISC_SET, this IC operates as follows.

■Outline

This function is installed to cancel the bridge change with time. A difference of the result between the two channels is stored as a result of one channel. The image of the difference mode operation is given below.

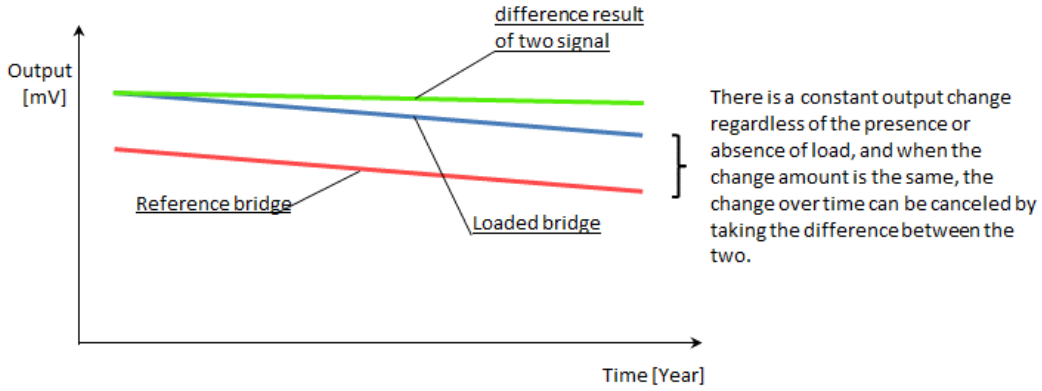


Fig. 15.3 Image of difference mode operation

■Operating condition

At Normal Mode

1) SET_DIFF = High
2) Two or three bits out of EN_1ST, EN_2ND, and EN_3RD specify physical sensor (channel 1 or 2)

If all of the above conditions are not satisfied, the difference mode is not activated and the AD conversion result before calculation is stored.

At Sequential Mode

1) SET_DIFF = High
2) SET_SEQ specify physical sensor (channel 1 or 2)

If all of the above conditions are not satisfied, the difference mode is not activated and the AD conversion result before calculation is stored.
And, it is necessary to retrieve physical value in Normal Mode before measuring physical value in Sequential Mode.

■Details of operation

Operation expression and its target at Normal mode are given below.

Expression: c = b − a
Target: a = The last but one physical sensor AD conversion result of Normal mode conversion results
: b = The last physical sensor AD conversion result of Normal mode conversion results

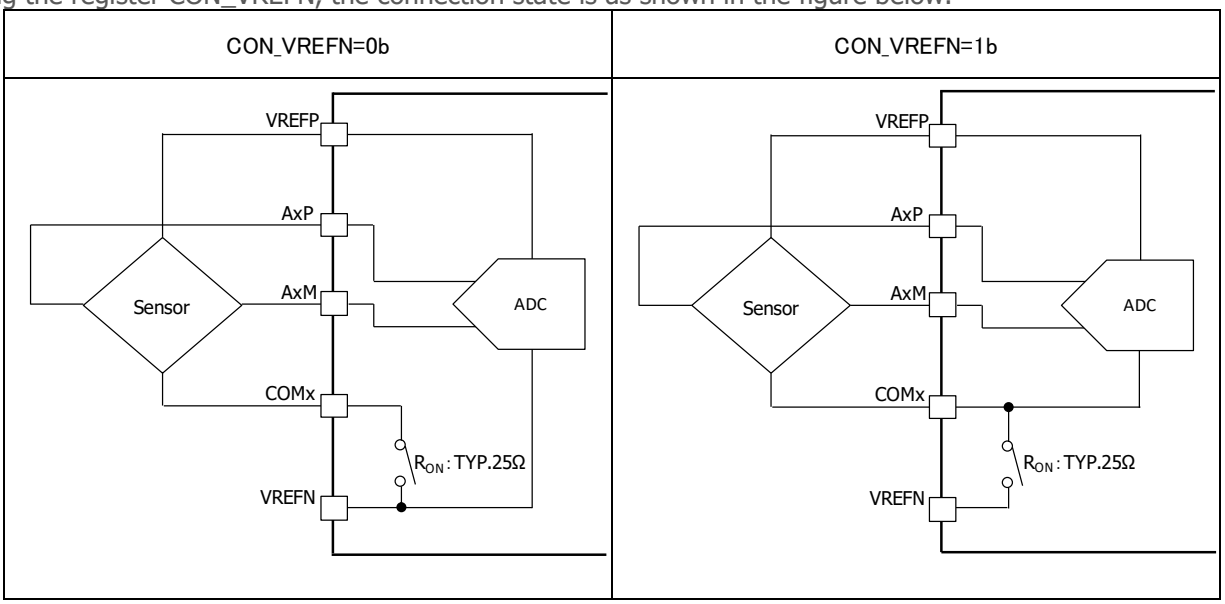
In the above case, the target corresponds to any of the following:
1) Result of channel specified in EN_2ND – Result of channel specified in EN_1ST
2) Result of channel specified in EN_3RD – Result of channel specified in EN_1ST
3) Result of channel specified in EN_3RD – Result of channel specified in EN_2ND
(Calculation when 3 channels of EN_1ST/2ND/3RD are set to physical sensor is 3).)

Operation expression and its target at Normal mode are given below.

Expression: c = b − a
Target: a = The last physical sensor AD conversion result of Normal mode conversion results acquired before Sequential Mode
: b = The physical sensor AD conversion result of Sequential Mode conversion result

In the above case, the target corresponds to any of the following:
1) Result of channel specified in SET_SEQ – Result of channel specified in EN_1ST
2) Result of channel specified in SET_SEQ – Result of channel specified in EN_2ND
3) Result of channel specified in SET_SEQ – Result of channel specified in EN_3RD

By setting the register CON_VREFN, the connection state is as shown in the figure below.



x=0, 1, 2

Fig. 15.4 The connection state by setting the register CON_VREFN

TRIM1/2/3/4 (Addr. = 5Eh～61h)

Table 15.24 Register address map (21/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
5Eh (TRIM1)	xxh	TRIM_LPVREF[3:0]				TRIM_LPOSC[3:0]				R/W
	DIGI _AON	TRIM_LPVREF [3:0]: Regulates regulator reference voltage for low power consumption. TRIM_LPOSC [3:0]: Regulates OCS oscillation frequency for low power consumption.								LV1/ LV3
5Fh (TRIM2)	xxh	Reserve		TRIM_BGR[5:0]						R/W
	DIGI _AON	TRIM_BGR [5:0]: Regulates BGR output voltage.								LV1/ LV3
60h (TRIM3)	xxh	TRIM_IREF[3:0]				TRIM_RG[3:0]				R/W
	DIGI _AON	TRIM_IREF [3:0]: Regulates reference current. TRIM_RG [3:0]: Regulates regulator output voltage during normal operation.								LV1/ LV3
61h (TRIM4)	xxh	SPD_OSC[1:0]		TRIM_OSC[5:0]						R/W
	DIGI _AON	SPD_OSC [1:0]: Rough regulates OSC oscillation frequency. TRIM_OSC [5:0]: Finely regulates OSC frequency.								LV1/ LV3

MON_SET (Addr. = 62h)

Table 15.25 Register address map (22/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
62h (MON_SET)	00h	DIS_FILT	Reserve	SEL_GPO[5:0]						R/W
	DIGI _AON	DIS_FILT: Specifies the input filter and output slope control of SCL/SDA terminal. 0: With filter and slope control 1: Without filter and slope control With filter, spike noise of up to 50ns width can be removed. With slope control, the rise / the fall time is 10 to 300ns. SEL_GPO [5:0]: Specifies GPO terminal. SEL_GPO [5:0]: 00_0100b: Outputs clock for TSTBY count. 00_1111b: Outputs main clock. 01_1000b: Outputs DRDY signal. 01_1001b: Outputs DRDYB signal. 10_0001b: Outputs BGR voltage. 10_0010b: Outputs IREF current. Other settings are made for TEST. DRDY (B) is a signal notifying completion of AD conversion data preparation.								LV1/ LV3

MISC_SET (Addr. = 63h)

Table 15.26 Register address map (23/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
63h (MISC _SET)	00h	SET_WARM	SET_ODET	SEL_CYC	EN_BI	TEST_ACT	SET_RGO[2:0]			R/W
	DIGI _AON	SET_WARM: Controls COM terminal switch. "0" is a standard setting and set the COM terminal switch to turns on only during State to convert AD. When "1" is set for state of Standby and Active, the COM terminal switch on all channels for AD conversion. SET_ODET: Controls sensor connection detection operation. "0" is a standard setting and is not activated the connection detection operation. When "1" is set, the connection detection operation activates after data transfer from NVM to REG during BootLoad. SEL_CYC : Controls of time for sensor connection detection. "0" is standard setting and Capacity to ground up to 100pF is assumed for use in an environment. This case, connection detection operation completes Max.4.0ms. When "1" is set, Capacity to ground up to 600pF is assumed for use in an environment. This case, connection detection operation completes Max.28.5ms. Bit[4:0] :For IC test Please specify these bits all "0".								LV1/ LV3

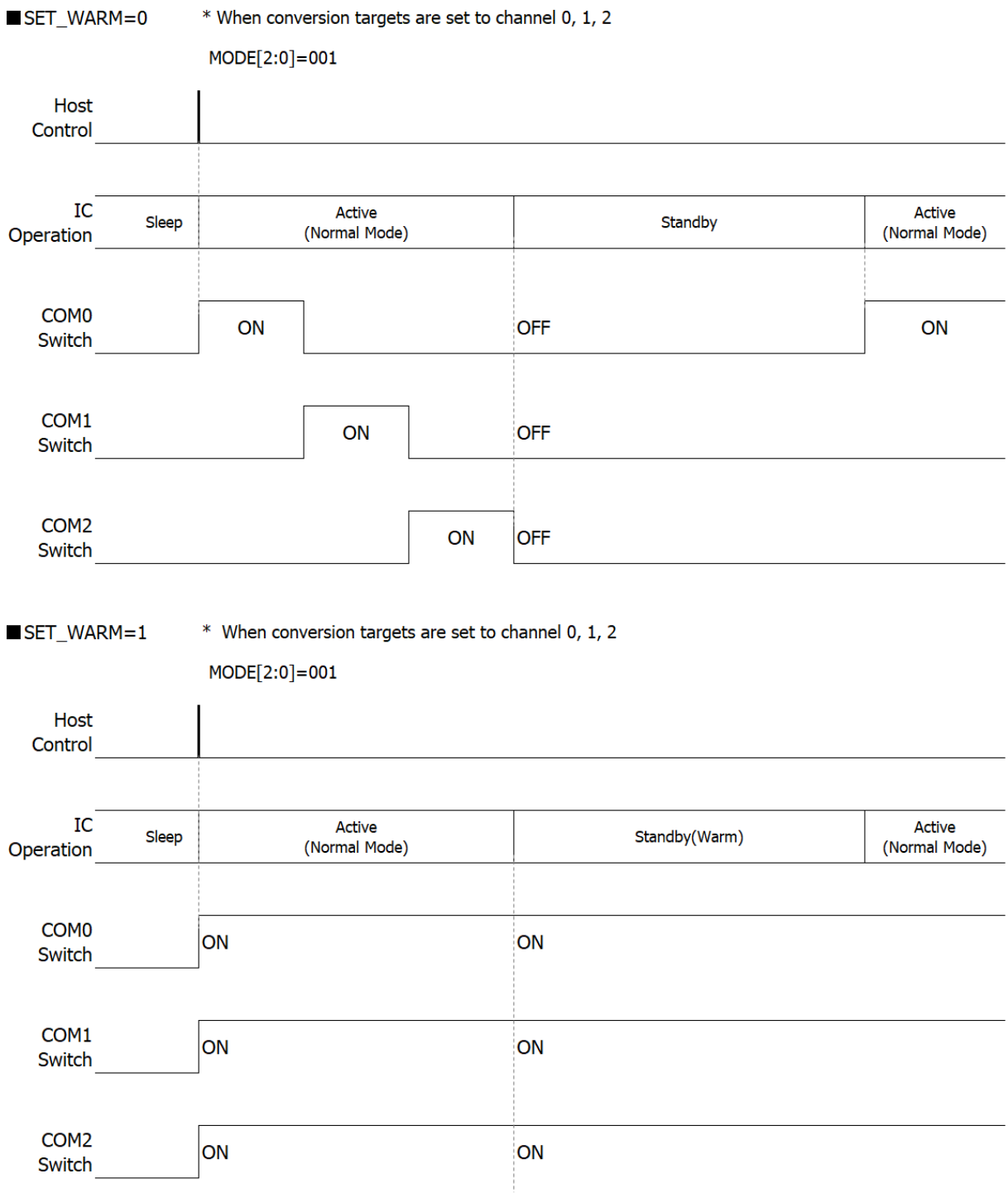


Fig. 15.5 Function of SET_WARM

NVM_TEST1/2 (Addr. = 64h～65h)

Table 15.27 Register address map (24/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
64h (NVM_TEST1)	00h	BULK_ODD_EN	BULK_EVEN_EN	MREAD_EN	CCMON_EN	OSCMON_EN	MARGIN_TRIM[2:0]			R/W
	DIGI_AON	For NVM TEST Details are separately described.								LV2/LV2
65h (NVM_TEST2)	00h	VTUNMON_EN	CORE_IBIAS_OVR_EN	OSC_OVR_EN	OSC_IBIAS_MON_EN	Reserve	DIS_CP	DIS_PROG	DIS_ERASE	R/W
	DIGI_AON	For NVM TEST Details are separately described.								LV2/LV2

ACCS_CTRL (Addr. = 66h)

Table 15.28 Register address map (25/25)

Address	Initial Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
66h (ACCS_CTRL)	00h	Reserve					EN_LV3	CTL_EN_LV3	EN_LV2	R/W
	DIGI_AON	Restricts register access. Setting of LV2 ① Reads this address. (Sends NACK after register address designation.) ② Writes the data 01h. (Sends NACK as well.) ③ Reads this address to confirm Data = 01h. (Confirms LV2 setting is applied.) Setting of LV3 ① Reads this address. (Sends NACK after register address designation.) ② Writes the data 01h. (Sends NACK as well.) ③ Reads this address. ④ Write the data 03h. ⑤ Reads this address. ⑥ Write the data 07h. In addition, after setting access restrict to LV3 by operating up to ⑥, you can read 05h as this address data.								Special

These are concrete communication formats to release the access restriction. Regarding ②, the slave sends NACK after the register address is designated. After that, when it receives Data = 01h, the data can be written to this IC.

Fig. 15.6 Access restriction release

NVM (Non-volatile memory)

MV3830 contains NVM (Non-volatile memory) in order to store trimming for analog circuit and sensor correction value. This has 16bits width, so it is necessary to access by 16bits width. This NVM operates with the main regulator output voltage as the supply voltage, and the high voltage for writing is covered with the built-in charge pump, it is not necessary to apply a high voltage from the outside.
You can write about 100 times.
Must be access to NVM after setting MV3830 to state of Idle and waiting for 2ms or more.

NVM Address map

In NVM, access restriction (Read, Write) is specified.
To read from / write to NVM, setting of bit [2:0] (Addr. = 66h) is needed.
This IC has checksum function to detect incorrect data in this memory area.
Checksum result is stored in Addr. = AFh. The checksum coverage is all data except for the one stored in AFh.

The table is shown on the following page. For details of each parameter, see Register map.

Table 16.1 NVM address map (1/3)

Address	15-8/ 7-0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Read	Write
80h	15-8	*Reserve*	I2C ADDR[6:0]							LV1	LV2
	7-0	*Reserve*	*Reserve*	*Reserve*	SET_CRC	SELF_CHK	CIC_OSRALL	IIR_COEF[1:0]		LV1	LV2
81h	15-8	SET_SEQ[1:0]		EN_3RD[1:0]		EN_2ND[1:0]		EN_1ST[1:0]		LV1	LV2
	7-0	*Reserve*	TSTBY[2:0]			*Reserve*	MODE[2:0]			LV1	LV2
		For details, see Register map. It is following that contents related to operations are different from those described in the register address map. When MODE [2:0] is set as below, it will shift to Sleep. 100b（Reset）、110b（BootLoad）									
82h	15-8	SET_GPOTH[1:0]	GPOTH_DATA[13:8]							LV1	LV2
	7-0	GPOTH_DATA[7:0]								LV1	LV2
83h	15-0	CC_CH0_Z[15:0]								LV1	LV2
84h	15-0	CC_CH0_F[15:0]								LV1	LV2
85h	15-0	CC_CH0_S[15:0]								LV1	LV2
86h	15-0	CC_CH0_T[15:0]								LV1	LV2
87h	15-0	CC_CH1_ZZ[15:0]								LV1	LV2
88h	15-0	CC_CH1_ZF[15:0]								LV1	LV2
89h	15-0	CC_CH1_ZS[15:0]								LV1	LV2
8Ah	15-0	CC_CH1_FZ[15:0]								LV1	LV2
8Bh	15-0	CC_CH1_FF[15:0]								LV1	LV2
8Ch	15-0	CC_CH1_FS[15:0]								LV1	LV2
8Dh	15-0	CC_CH1_SZ[15:0]								LV1	LV2
8Eh	15-0	CC_CH1_SF[15:0]								LV1	LV2
8Fh	15-0	CC_CH1_SS[15:0]								LV1	LV2
90h	15-0	CC_CH1_TZ[15:0]								LV1	LV2
91h	15-0	CC_CH1_TF[15:0]								LV1	LV2
92h	15-0	CC_CH1_TS[15:0]								LV1	LV2

Table 16.2 NVM address map (2/3)

Address	15-8/ 7-0	Init. Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Read	Write
93h	15-0	xxxxh	CC_CH2_ZZ[15:0]								LV1	LV2
94h	15-0	xxxxh	CC_CH2_ZF[15:0]								LV1	LV2
95h	15-0	xxxxh	CC_CH2_ZS[15:0]								LV1	LV2
96h	15-0	xxxxh	CC_CH2_FZ[15:0]								LV1	LV2
97h	15-0	xxxxh	CC_CH2_FF[15:0]								LV1	LV2
98h	15-0	xxxxh	CC_CH2_FS[15:0]								LV1	LV2
99h	15-0	xxxxh	CC_CH2_SZ[15:0]								LV1	LV2
9Ah	15-0	xxxxh	CC_CH2_SF[15:0]								LV1	LV2
9Bh	15-0	xxxxh	CC_CH2_SS[15:0]								LV1	LV2
9Ch	15-0	xxxxh	CC_CH2_TZ[15:0]								LV1	LV2
9Dh	15-0	xxxxh	CC_CH2_TF[15:0]								LV1	LV2
9Eh	15-0	xxxxh	CC_CH2_TS[15:0]								LV1	LV2
9Fh	15-8	xxxxh	BITSHIFT_CH0_F[3:0]				BITSHIFT_CH0_S[3:0]				LV1	LV2
	7-0		BITSHIFT_CH0_T[3:0]				BITSHIFT_CH1_ZF[3:0]				LV1	LV2
A0h	15-8	xxxxh	BITSHIFT_CH1_ZS[3:0]				BITSHIFT_CH1_FF[3:0]				LV1	LV2
	7-0		BITSHIFT_CH1_FS[3:0]				BITSHIFT_CH1_F[3:0]				LV1	LV2
A1h	15-8	xxxxh	BITSHIFT_CH1_SF[3:0]				BITSHIFT_CH1_SS[3:0]				LV1	LV2
	7-0		BITSHIFT_CH1_S[3:0]				BITSHIFT_CH1_TF[3:0]				LV1	LV2
A2h	15-8	xx0xh	BITSHIFT_CH1_TS[3:0]				BITSHIFT_CH1_T[3:0]				LV1	LV2
	7-0		*Reserve*	*Reserve*	*Reserve*	*Reserve*	BITSHIFT_CH2_ZF[3:0]				LV1	LV2
A3h	15-8	xxxxh	BITSHIFT_CH2_ZS[3:0]				BITSHIFT_CH2_FF[3:0]				LV1	LV2
	7-0		BITSHIFT_CH2_FS[3:0]				BITSHIFT_CH2_F[3:0]				LV1	LV2
A4h	15-8	xxxxh	BITSHIFT_CH2_SF[3:0]				BITSHIFT_CH2_SS[3:0]				LV1	LV2
	7-0		BITSHIFT_CH2_S[3:0]				BITSHIFT_CH2_TF[3:0]				LV1	LV2
A5h	15-8	xx00h	BITSHIFT_CH2_TS[3:0]				BITSHIFT_CH2_T[3:0]				LV1	LV2
	7-0		*Reserve*	*Reserve*	*Reserve*	*Reserve*	*Reserve*	SEL_RAW	SET_STAT	DIS_RES_WIDTH	LV1	LV2
A6h	15-8	xxxxh	TRIM_VOFF1[7:0]								LV1	LV2
	7-0		TRIM_VOFF2[7:0]								LV1	LV2
A7h	15-8	0000h	CH0_OSR[1:0]		CH0_AVG[2:0]			CH0_GAIN[2:0]			LV1	LV2
	7-0		CH1_OSR[1:0]		CH1_AVG[2:0]			CH1_GAIN[2:0]			LV1	LV2
A8h	15-8	0010h	CH2_OSR[1:0]		CH2_AVG[2:0]			CH2_GAIN[2:0]			LV1	LV2
	7-0		*Reserve*	DIS_DEM_PGA	SET_DIFF	CON_VREFN	CH2_TYPE	CH1_TYPE	CH0_DISCON	CH0_SEL_EXTEMP	LV1	LV2

Table 16.3 NVM address map (3/3)

Address	15-8/ 7-0	Init. Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Read	Write
A9h	15-8	xxxxh	TRIM_LPVREF[3:0]				TRIM_LPOSC[3:0]				LV1	LV2
	7-0		*Reserve*	*Reserve*	TRIM_BGR[5:0]						LV1	LV2
AAh	15-8	xxxxh	TRIM_IREF[3:0]				TRIM_RG[3:0]				LV1	LV2
	7-0		SPD_OSC[1:0]		TRIM_OSC[5:0]						LV1	LV2
ABh	15-8	0000h	DIS_FILT	*Reserve*	SEL_GPO[5:0]						LV1	LV2
			For details, see Register map. The value set in the register at BootLoad differs depending on the setting value of bit5(SEL_GPO[5]). 0b : SEL_GPO[5:0] = bit[5:0] are set in the register at BootLoad. 1b : SEL_GPO[5:0] = 00h are set in the register at BootLoad.									
	7-0		SET_WARM	SET_ODET	SEL_CYC	0	0	0	0	0	LV1	LV2
ACh	15-8	xxxxh	Result of probe inspection								LV1	LV2
			It is stored the result of probe test.									
	7-0		Result of post assembly inspection								LV1	LV2
			It is stored the result of post assembly inspection.									
ADh	15-8	xxxxh	Lot number								LV1	LV2
			It is stored the lot number of wafer.									
	7-0		Wafer number								LV1	LV2
			It is stored the wafer number.									
AEh	15-8	xxxxh	CHIP_X[7:0]								-	-
			It is stored the X coordinate of wafer. It is the 100 minuse value from the prober coordinate.									
	7-0		CHIP_Y[7:0]								-	-
			It is stored the Y coordinate of wafer.									
AFh	15-0	xxxxh	CRC16CCITT[15:0]								-	-
			It is stored checksum.									

Method to calculate CRC check sum value

To detect incorrect data written in the NVM, MV3830 has a region to write a CRC check sum value. Specifications for CRC check sum are given below.

Table 16.4 Specifications for NVM data CRC check sum

Item	Description
Check target	NVM data（Addr.=80h～AEh）
Name	CRC16-CCITT
Polynomial	$x^{16} + x^{12} + x^5 + 1$
Initial value	16'hFFFF
Shift	Left shift
Output inversion	no

A logical product of an operation result and an initial value is calculated. To shift bits to the left, the LSB of the operation result is calculated from the input data and the entire operation result is left-shifted. If the MSB is 1 at the shift, generator polynomial is added for each bit (XOR of the operation result and the generator polynomial is calculated). This is repeated as many times as the number of input bits. The calculation result when it is completed is the CRC value.

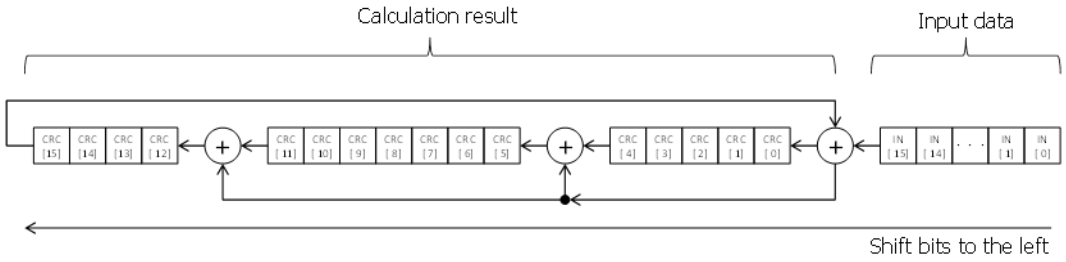
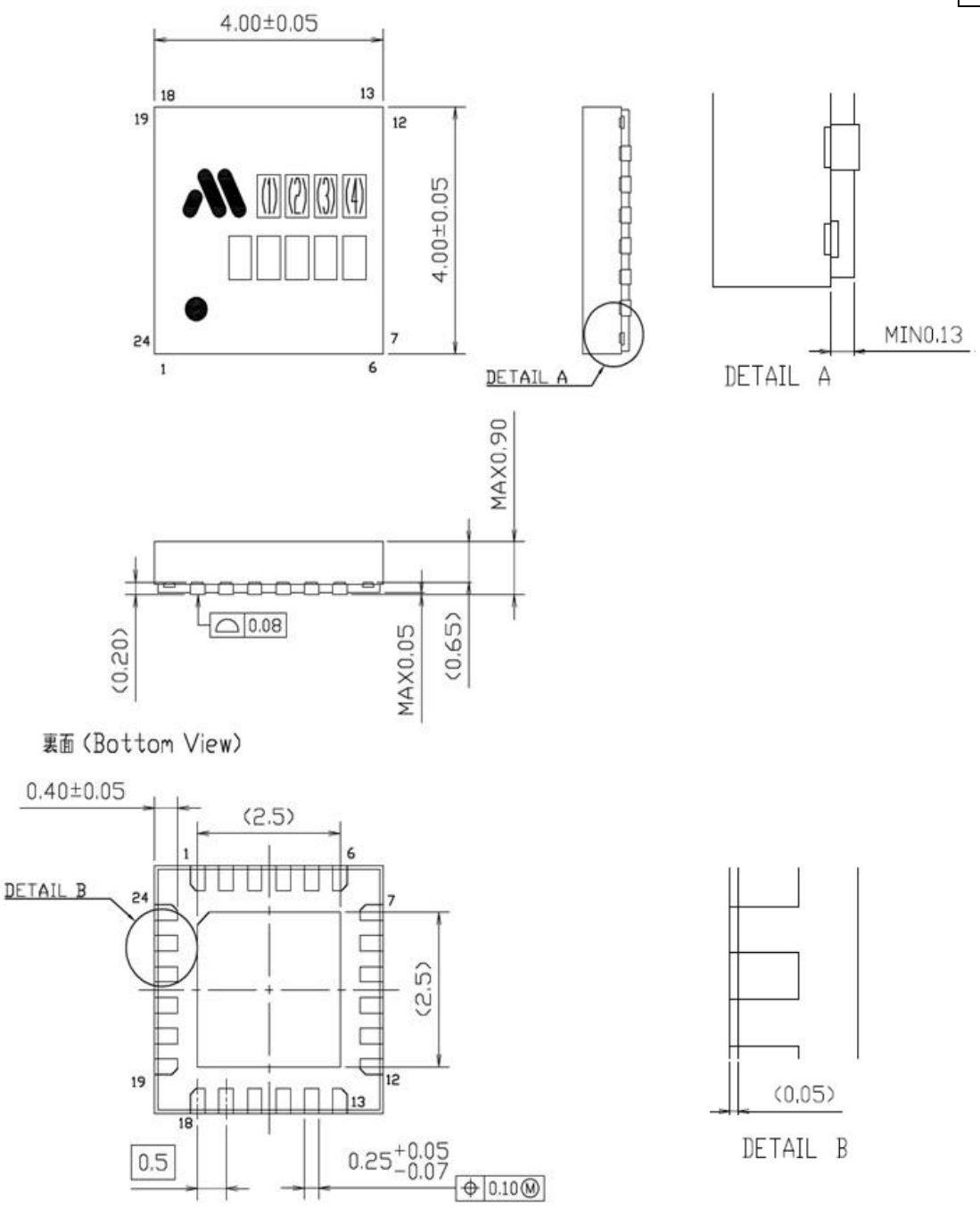


Fig. 16.1 CRC calculation

DIMENSIONS

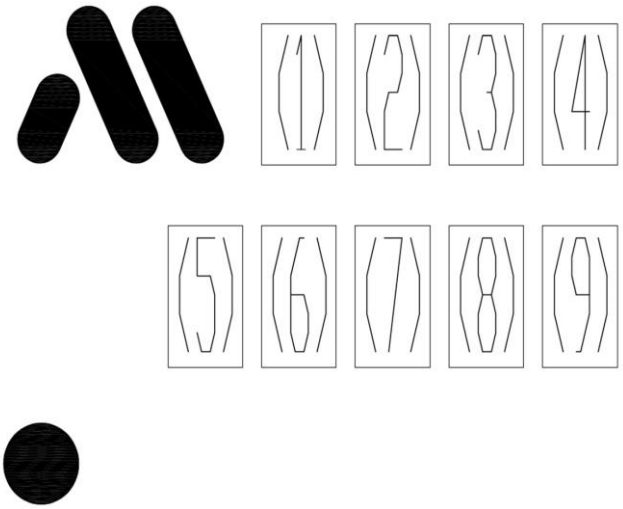
PACKAGE: SQFN-24C

UNIT	mm



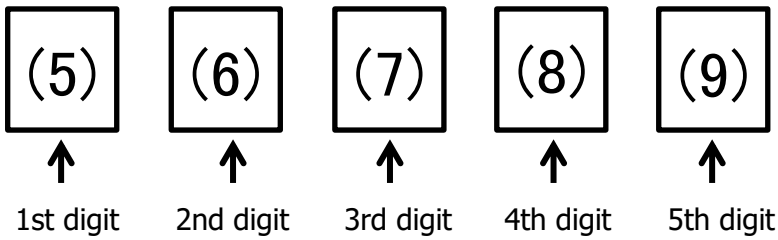
No. R24-SQFN24C-0002

MARKING CONTENTS



Model name	Model No.			
	(1)	(2)	(3)	(4)
MV3830ARREG2	3	8	3	0

How to identify 5 characteristic lot numbers.



1. The 1st (5) and 2nd (6) digit shows the last 2 digit of a production year (western calendar).
2. The 3rd (7) and 4th (8) digit show a production week of mass production.
3. The 5th (9) digit show a wafer lot.

【How to indicate a production year】

The 1st digit (5)	
the last digit of a production year	mark
xx1x	1
xx2x	2
xx3x	3
xx4x	4
xx5x	5
xx6x	6
xx7x	7
xx8x	8
xx9x	9
xx0x	0

The 2nd digit (6)	
the last digit of a production year	mark
xxx1	1
xxx2	2
xxx3	3
xxx4	4
xxx5	5
xxx6	6
xxx7	7
xxx8	8
xxx9	9
xxx0	0

The 3rd and 4th digit (7)(8)			
production week	mark	production week	mark
1	01	27	27
2	02	28	28
3	03	29	29
4	04	30	30
5	05	31	31
6	06	32	32
7	07	33	33
8	08	34	34
9	09	35	35
10	10	36	36
11	11	37	37
12	12	38	38
13	13	39	39
14	14	40	40
15	15	41	41
16	16	42	42
17	17	43	43
18	18	44	44
19	19	45	45
20	20	46	46
21	21	47	47
22	22	48	48
23	23	49	49
24	24	50	50
25	25	51	51
26	26	52	52
		53	53

NOTES

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